

Central Signal Processor Requirements Specification

020.40.00.00.00-0001 REQ Status: **RELEASED**

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1 Introduction

1.1 Purpose

This document presents the complete set of Level 2 subsystem requirements that guide the design and development of the Central Signal Processor (CSP) subsystem. Requirements described in this document are derived from applicable ngVLA System Requirements and System-Level Specification documents as listed in the Applicable Documents table. The engineering process and requirements hierarchy that govern this specification are defined in [\[AD01\]](#page-6-4) and [\[AD02\]](#page-6-5) respectively.

The content of these requirements is at the subsystem level, conforming to the system architecture [\[AD06\]](#page-6-6), but aims to be implementation agnostic within the subsystem boundaries. Some assumptions about the subsystem may be given, but only to the degree necessary to unambiguously define the subsystem requirements.

1.2 Scope

The scope of this document is to delineate the specifications for the Central Signal Processor (CSP) subsystem, specifically identified by configuration item number 020.40.00.00.00. Historically, the CSP functionally included the antenna Digital Back End (DBE), denoted by configuration number 020.30.25.00.00. However, due to a distinct functional partition between the DBE and CSP, the DBE is no longer considered within the CSP's functional domain. It is noteworthy that this set of requirements still incorporates functional aspects related to the DBE, which will be excluded in future versions, with clear identification of these requirements slated for removal. The document's scope encompasses:

- Assumptions on which the requirements are based.
- Definition of environmental conditions to be used in the definition of requirements.
- A complete set of requirements for the subsystem needed for the development, operation and maintenance of the subsystem, including interface requirements that are derived from the applicable list of ICDs.
- Numbering of all requirements and establishment of traceability to higher level requirements.
- Verification requirements and their traceability to the subsystem main requirements.
- Identification of Key Performance Parameters (KPPs) at the subsystem level.

The Level 2 Subsystem Requirements, along with detailed explanatory notes, are found in Section [8.](#page-18-4) The notes contain elaborations regarding the meaning, intent, and scope of the requirements. These notes form an important part of the definition of the requirement. In many cases, the notes contain an analysis of how the numeric values of requirements were derived to ensure correct interpretation of the requirements and to resolve ambiguity.

In cases where the requirements analysis is incomplete, such values are marked with TBD or TBC, which need to be resolved before the final specification is published.

2 Related Documents and Drawings

2.1 Applicable Documents

The following documents apply to this Requirements Specification to the extent specified. In the event of a conflict between the documents referenced herein and the content of this Requirements Specification, the content of the highest-level specification (in the requirements flow-down) shall be considered the superseding requirement for design elaboration and verification.

2.2 Applicable ICDs

The following Interface Control Documents define the external boundary of this subsystem and are applicable to its specification:

Note that the ICDs listed above have not yet been developed as of the time of writing. Therefore, many of the associated requirements are preliminary or basic placeholders. Interfaces are within the scope of the Preliminary Design phase, and as such, they will be presented for review during the PDR.

2.3 Reference Documents

The following documents are referenced within this text or provide supporting context:

3 Definitions

The terms listed below have precise definitions and are consistently utilized throughout this document. These definitions are aligned with those provided in the ngVLA Lexicon [\[RD10\]](#page-7-2), and any discrepancies between definitions shall defer to the definitions provided herein.

POLARIZATION PRODUCT: The correlation between the signals received by pairs of antennas with either the same (co-polarization products) or different antenna polarizations (cross-polarization products). Polarization products encompass various combinations such as XX, XY, YX, and YY for linearly polarized antennas, or RR, RL, LR, and LL for circularly polarized antennas.

SUBARRAY: A subarray is a set of antennas reserved for exclusive control that may be allocated one or more independent sets of processing resources in order to produce one or more data product streams. This definition has been harmonized at the system level and is uniformly applied across subsystems. One implication of this definition is that all CSP configuration parameters must be independently adjustable for different subarrays.

SUBBAND: In this document, the term 'subband' denotes one of the numerous digital signals received at the CSP input from the Digital Back End (DBE). The DBE partitions the digitizer output into frequency channels, known as subbands, which are subsequently chosen individually for additional processing and transmitted to the Central Electronics Building housing the CSP. Typically, a subband corresponds to the associated polarization pair, unless explicitly stated otherwise. Although bandwidth selection flexibility may impose constraints on the subband bandwidth, this bandwidth is ultimately a system design parameter determined by considering multiple trade-offs between the DBE and CSP designs. Therefore, this requirements specification does not specify the subband bandwidth.

4 Overview of Subsystem

4.1 Subsystem Boundary, Context, and External Interfaces

The Central Signal Processor (CSP) is the component of the ngVLA responsible for processing digital signals received from each antenna's Digital Back End (DBE) and generating raw data products¹ on a persubarray basis. Depending on the subarray configuration, the CSP generates various data products, including visibilities, average pulse profiles, full-Stokes time-series data, and beamformed digital voltage for data recorders. The CSP receives digital signals from each antenna with a total bandwidth specified in CSP0008 (a minimum of 14 GHz), which is divided into multiple subbands. Each subband, received in the form of a time-stamped time series, represents a frequency channel generated and downselected by the DBE from the digitized spectrum. These subbands have a bandwidth of 218.75 MHz and are sampled at 250 MHz. They may cover non-contiguous portions of the frequency spectrum. Subbands are created by splitting the output of the digitizer into frequency subbands and then undergo preprocessing by the DBE for receiver calibration, addressing non-idealities such as I/Q imbalance compensation.

[Figure 1](#page-9-2) represents the product context of the CSP through its Systems Modelling Language (SysML) context diagram. All the CSP equipment is located at the Central Electronics Building (CEB) within the ngVLA Site Buildings subsystem (NSB, CI number 020.61.10.00.00). The NSB subsystem provides the CSP with power, HVAC room cooling, physical space, and RFI shielding [\[AD21\]](#page-6-7).

The Central Fiber Optic (FIB) subsystem, identified by CI number 020.55.20.00.00, encompasses the optical fiber infrastructure. It plays a crucial role in facilitating the transmission of data from the DBE to

¹ By 'raw' data products, it is meant that calibrations performed offline will be carried out downstream by the Computing and Software System (CSS).

the CSP by providing the physical interface between the two components, as outlined in the corresponding Interface Control Document (ICD) [\[AD24\]](#page-6-8).

Figure 1 – Central Signal Processor product context.

In the context of the CSP, the LO Reference and Timing Generation subsystem (RTG, CI number 020.35.05.00.00) serves the function of providing the CSP with timing information synchronized to the central ngVLA time. This ensures precise timing coordination across the system. While the use of RTG is one approach to achieve this synchronization, alternative designs may opt to utilize Precision Time Protocol (PTP) servers for the same purpose.

Data products generated by the CSP are sent to the Computing and Software System (CSS, CI number 020.50.00.00.00), specifically its Online Data Acquisition sub-element (ONL, CI number 020.50.10.00.00) [\[AD23\]](#page-6-9). The Monitoring & Control subsystem (MCL, CI number 020.50.25.00.00) and the Technical Infrastructure (TI, CI number 020.50.20.00.00) of the CSS also interface with the CSP at various levels [\[AD22,](#page-6-10) [AD25\]](#page-6-11).

4.2 Subsystem Functional Overview

The functional overview of the CSP is better understood from the respective functional overviews of its component parts.

After receiving the digitized data from the IRD modules, the DBE applies a calibration filter on the received signal in order to equalize the spectrum and further suppress the unwanted sideband from the down conversion process, effectively performing sideband separation digitally. Then, a frequency shifter coarsely tunes the digitized spectrum and removes any per-antenna LO-shift as needed. After that, the bandwidth is split into frequency subbands through a filter bank. Finally, the selected subband data streams undergo a requantization process and the resulting data packets are timestamped for its transmission to the SBP.

The SBP has the capability to perform 4 differentiated task which are independently configured for each subarray depending on the observation mode:

- 1. Delay and Phase Tracking
- 2. Fine Frequency Channelization
- 3. Beamforming (Linear Combination)
- 4. (Cross-)Correlation

For example, as the SBP follows the so-called FX architecture in interferometric modes, it performs tasks 1, 2 and 4, in that order. In beamforming modes, task 4 is not carried out. The following figures depict the functional diagram of all 4 tasks of the SBP, which are then briefly described. More details can be found in the SBP requirements and design documents [\[RD07](#page-7-3)[,RD08\]](#page-7-4).

Figure 2 – Functional diagram of the delay and phase tracking task of the SBP.

Figure 3 – Functional diagram of the fine frequency channelization task of the SBP.

Figure 4 – Functional diagram of the beamforming task of the SBP.

Figure 5 – Functional diagram of the correlation task of the SBP.

displays the SBP's delay and phase tracking function for each subband data stream from the DBE, involving reception, sorting, and storage of antenna data. The process corrects bulk delay, applies fine sub-sample delay through resampling, and introduces time-variable phase correction before transitioning to the fine frequency channelization function. While fine delay correction can be executed in the frequency domain, it may incur correlation loss depending on frequency resolution. However, the need to rectify sampling frequency offsets introduced at the antenna necessitates the use of a resampler. Thus, integrating fine delay corrections within the resampling process proves advantageous.

In , the SBP's fine frequency channelization is illustrated to split subband data into precise frequency channels for beamforming or correlator input. The function employs spectral zoom modes, allowing selective tuning and downsampling to achieve the finest frequency resolution. Data is then prepared for beamforming or correlation through requantization, data rearrangement, and packetization.

outlines the beamformer's functional diagram, showcasing multiple processing units for subarray signal combination. Starting with synchronization and polarization correction, signals are linearly combined based on defined coefficients. The resulting synthetic signal is requantized and prepared for transmission to the CSP Back End (CBE).

Finally, details the correlation function, collecting data from antennas via the fine frequency channelizer. A complex multiply-and-accumulate operation is executed, and short timescale visibilities are flagged for RFI. The produced data is then transmitted to the CBE for further processing and archiving.

4.3 Design Driving Requirements

The following table provides a summary of the major design-driving subsystem requirements. Should there be a conflict between the requirements listed here and the descriptions in Section [8,](#page-18-4) the latter shall take precedence. Refer to Section [8](#page-18-4) for further details and a justification for these requirements.

5 Requirements Management

5.1 Requirements Definitions

Consistent with the Requirements Management Plan [\[AD02\]](#page-6-5), the following definitions of requirement "levels" are used in the ngVLA program. The requirements in this document are at the L2 subsystem level.

5.2 Requirements Flow Down

[Figure 6](#page-15-3) shows the relationships between the CSP subsystem (L2) requirements and the System (L1) Requirements from which they are derived. System Requirements include Security, Safety, and Environmental Specifications that apply to the CSP. They also include EMC and RFI Mitigation requirements. In an intermediate level between System and CSP requirements (L1.1), Electronics, Calibration and Technical Budgets requirements have been derived from the System Requirements and are applicable to the CSP subsystem as well.

Individual subsystem specifications (Level 2) flow from the Level 1 requirements and may not always be directly attributable to a single system requirement. For example, phase drift specifications at the system level may be apportioned to multiple subsystems, or a subsystem spec may be in support of multiple higher-level requirements. Completeness of the Level 2 requirements is assessed at the requirements review of each subsystem.

While this is a top-down design process, the process is still iterative rather than a "waterfall" or linear process. The feasibility and cost of requirements implementation lead to trade-offs that feedback to higherlevel requirements. The end goal is to build the most generally capable system that will support the Key

Science Goals within the programmatic constraints of cost and schedule. Maintaining enumerated traceability between system requirements and subsystem requirements ensures that this trade-off process can be managed in a controlled way.

Figure 6 – Requirements flow-down to the Central Signal Processor Subsystem Requirements.

5.3 Verb Convention

This document uses "shall" to denote a requirement. The verbs "should" and "must" denote desired but not strictly required parameters. "Will" denotes a future happening. Desired but not required features are noted as "desirable" or "goals."

6 Assumptions

The following assumptions are made in the definition of these subsystem requirements:

- 1. Subsystem requirements apply to performance before any operational calibration corrections are applied unless explicitly stated otherwise.
- 2. Hardware requirements are applicable to a system functioning properly under normal operating environmental conditions, as defined in Section [7.1,](#page-16-1) unless explicitly stated otherwise.
- 3. Hardware requirements assume that all system parts that would normally be in place during observations are working within their respective specifications (e.g., HVAC, RTP system) unless explicitly stated otherwise.
- 4. Environmental requirements assume the antenna sites and ngVLA buildings are designed to host all corresponding CSP elements.

- 5. Functional requirements assume the CSP architecture represented in , where the subband bandwidth is fixed.
- 6. Functional requirements assume filter-bank based frequency channelizers in the down-selection of the processed bandwidth.
- 7. The system requirements specify a correlation loss of 5% for the overall digital system, which includes the antenna digitizer, Digital Back End (DBE), and Central Signal Processor (CSP). The distribution of this loss among these components is left to the system designer. In this requirements specification, the following allocation is assumed: 0.6% correlation loss for the CSP, 4% for the digitizer, and 0.4% for the DBE. This assumption is based on the headroom available at the digitizer [\[RD13\]](#page-7-6), as well as the expected performance of the CSP and DBE designs.
- 8. The computation and application of the quantization correction are the responsibility of the Computing and Software System (CSS). However, the CSP will provide total power information as needed to compute these corrections.
- 9. Delay and phase model parameters are calculated by the Computing and Software System (CSS) subsystem and provided to the CSP. Thus, the CSS is responsible for compliance with System Requirements [\[AD03\]](#page-6-12) in this regard, e.g., OTF mapping.
- 10. The delay and phase model parameters provided by the CSS include terms for the compensation of the drift of the antenna time standard with respect to the central time standard. The timestamping accuracy of the CSP is specified and validated assuming ideal (error-free) parameter inputs.
- 11. Beamforming coefficients are computed by the CSS. Hence, the ultimate responsibility for generating nulling directions and controlling side lobes resides in the CSS.
- 12. The support of per-baseline integration times does not include the CSP.
- 13. The CSP is not responsible for recording the failure of its items in a FRACAS (Failure Reporting, Analysis, and Corrective Action System).

7 Environmental Conditions

7.1 Normal Operating Conditions

All CSP equipment shall be installed in environmentally controlled facilities or racks. As such, the normal operating conditions are defined by the applicable ICD:

• [\[AD21\]](#page-6-7) 020.10.40.05.00-0098 ngVLA Site Buildings–Central Signal Processor Interface Specification

This ICD leads to the corresponding CSP requirements, as defined by CSP subsystem interface requirements in Section [8.2.1.](#page-35-1)

The requirements in this section are derived directly from the system environmental specification [\[AD04\]](#page-6-13) and, in some cases, necessitate specific verification methods. However, subjecting all CSP equipment to environmental testing could be costly and add minimal value. Therefore, these requirements may be relaxed in future releases for Commercial Off-The-Shelf (COTS) equipment.

7.2 Transportation Conditions

CSP9001 is a placeholder for future transportation conditions requirements.

CSP9007 is a copy of the system environmental specification ENV0531. See [\[AD04\]](#page-6-13) for additional details and rationale.

CSP9008 is a copy of the system environmental specification ENV0582. See [\[AD04\]](#page-6-13) for additional details and rationale.

7.3 Storage Conditions

CSP9002 is a placeholder for future storage conditions requirements.

7.4 Site Elevation

The CSP, located at the CEB, does not need to operate at higher altitudes.

7.5 Environmental Protection Requirements

7.5.1 Seismic

The elements of the CSP shall not sustain residual damage under these conditions while in the installed and operational state. CSP9004 is a copy of system environmental specification ENV0521. See [\[AD04\]](#page-6-13) for additional details and rationale.

7.5.2 Vibration

CSP9005 is only applicable to the DBE, and hence does not apply to the CSP. CSP9005 is kept only for legacy purposes and will be removed in future releases. All DBE elements must meet ENV0531.

7.5.3 Mechanical Shock

No mechanical shock levels have been defined for the survival of the CSP LRUs when not packaged for transportation. See Section [7.2](#page-16-2) for the shock levels defined for transportation conditions.

7.5.4 Lightning, Dust, Fauna, Solar Radiation, Rain/Water Infiltration, & Corrosion Protection

Protection against lightning, dust, fauna, solar radiation, rain/water infiltration and corrosion shall be provided by the environmentally controlled facilities in which the CSP elements are installed, as defined by the applicable ICD, [\[AD21\]](#page-6-7). No CSP element shall be installed outside these facilities.

7.5.5 Cosmic Radiation

CSP9006 is currently a placeholder for potential future requirements. It will be replaced by clearer, more verifiable requirements, as its current form lacks verifiability due to the undefined nature of 'best practices' associated with it. Note that SEUs affect FPGA devices much more severely than ASICs.

8 Subsystem Requirements

8.1 Functional and Performance Requirements

8.1.1 Operating Mode Requirements

The above Operating Mode Requirements provide a simple overview of the different functionality required from the CSP, grouped by the nature of the data product. Different Operating Modes demand different functional and performance requirements. Such requirements are specified in the following sections. The CSP design can develop as many functional modes as needed to fully cover the functional and performance parameter space.

System's Interferometric, Total Power, and On-The-Fly Mapping Modes govern the interferometric capabilities of the CSP; System's Phased Array and VLBI Modes define the beamforming capabilities of the CSP; and System's Pulsar Timing and Pulsar and Transient Search Modes are supported by the Pulsar Timing and Search capabilities of the CSP, respectively.

CSP0004 is currently a placeholder for future, more specific requirements. The 10-second allocation is for the entire ngVLA system, and it is not yet clear what the CSP's allocation will be in the reconfiguration time budget. Additionally, CSP0004 will likely be developed into different use cases, each with varying time allocations depending on the specific system requirements.

CSP0005 defines Standby Mode as the default mode. This default mode is the functional mode to which the CSP must revert in the absence of a proper functional mode command. The intended granularity of the standby mode is on a per-Line Replaceable Unit (LRU) basis, meaning that LRU resources not actively participating or allocated to any specific subarray are in 'standby' mode or a similar state, thereby minimizing power consumption.

8.1.2 General Functional and Performance Requirements

The computational requirements of the CSP are determined by the number of antennas and the processed instantaneous bandwidth. To ensure long-term value, it is preferred that the CSP architecture is inherently scalable to accommodate any number of antenna inputs or receiver bandwidth. This not only mitigates the risk of future hardware upgrades lacking sufficient value to justify the replacement of old hardware but also supports the gradual deployment of the CSP in multiple phases and allows for graceful degradation of the system in the event of malfunction.

CSP0006 and CSP0010 emanate from the current array configuration. This configuration concept defines a 263-antenna ngVLA, arranged as 214 antennas for the main array, 19 antennas for the SBA (Short Baseline Array), and 30 antennas for the LBA (Long Baseline Array). The preferred design will be scalable to any given number of antennas, as opposed to a constrained architecture.

Finally, CSP0006 currently does not incorporate provisions for 'spare' or additional antenna inputs. Firstly, antenna inputs are not hardwired to CSP computational resources, allowing for the possibility of connecting new antennas simply to the CSP input switched fabric. Secondly, while scalability is not an official requirement, it is a characteristic shared by all designs considered for the CSP. Lastly, the exact allocation of spare inputs remains undetermined. Nonetheless, supporting at least a 5% increase (equivalent to 13 additional antennas) is considered sufficient.

While not directly influencing the CSP architecture, this requirement serves as the basis for deriving additional CSP specifications by defining the system's minimum and maximum radio frequencies.

The maximum bandwidth processed in each Operating Mode is determined by the non-redundant bandwidth transmitted from every antenna (CSP0008). Within the ngVLA system, the CSP processes several DBE subbands, collectively constituting the processed bandwidth. The DBE, situated at the antenna, downselects a subset of subbands, which may or may not align with the subbands of a sideband. Consequently, CSP0008 does not specify the bandwidth per sideband.

However, it is important to note that the CSP is not required to process all available bandwidth in every Operating Mode. Additional constraints, such as simultaneous subarray operation or specific Operating Modes, may limit the amount of bandwidth processed, as detailed in subsequent sections. Nonetheless, there is potential for processing up to 20 GHz of bandwidth in any Operating Mode in the future [\[RD03\]](#page-7-7), underscoring the rationale behind striving for a scalable design.

Correlation loss will be measured using a predefined set of use cases, as specified in Section 10.2. One such case involves a white (flat spectrum) Gaussian signal and noise with moderate SNR, measured over the bandwidth of a subband.

System requirement SYS1033 sets an overall correlation loss of 5% for the 'digital system.' This digital system encompasses 3 distinct components, the digitizer and the Digital Back End at the antenna, as well as the CSP in the Central Electronics Building. In CSP0009, the CSP correlation loss assumes a digitizer correlation loss of 4% and 0.4% for the DBE, aligning with the current system technical budget for digital correlation loss [AD10]. Digital correlation losses typically occur when data are approximated by their finite precision representation, which can include various parameters such as signals, delays, phases, (filter) coefficients, or correlation estimates.

While this requirement formally applies only in interferometric mode, it might impact the common perantenna processing chain of all operating modes and is therefore included with general requirements.

CSP0009 applies to all frequencies within the system frequency span defined by SYS0803, SYS0804, and SYS0805. The CSP frequency channelization strategy must ensure this requirement can be fulfilled without gaps in frequency coverage. For instance, adequate spectral overlap across subbands must be allocated so that frequency channels at the subband edges failing to meet CSP0009 criteria are discarded, while adjacent subbands meet CSP0009 for the corresponding RF band.

A correlation loss budget for the CSP will be included within the CSP Design Description document [\[RD01\]](#page-7-5).

While data processing within the CSP is discrete-time, subsample delay correction may introduce additional frequency-dependent uncertainty in signal timing. This error must align with the System Technical Budgets [\[AD10\]](#page-6-15). Currently, the maximum overall system error, as per SYS2002, is 10 ns, with a target of 1 ns. It is anticipated that any random timing errors introduced by the CSP will be negligible compared to this, and any systematic timing error can be corrected in post-processing.

CSP0013 serves as a placeholder requirement. Future specifications will establish the maximum quantization error during the application of polarization corrections or transformations.

Commensal Signal Processors defined in CSP0014 are inherently supported by the assumed CSP architecture, but it must be enabled by supporting multicast capabilities.

This applies to spurious signals other quantization noise. It does not account for ill-posed cases, such as the system noise level well below one quantization step.

Ideally, any amplitude and delay/phase variations introduced by the CSP should be perfectly known. However, some time-varying processes such as delay or phase tracking may introduce small amplitude or delay/phase variations that change with time scales much smaller than the correlator accumulation period. Under those circumstances, tracking and compensating for such fast-paced variation becomes unwieldy. The main purpose of CSP0061 is to limit the contribution of the CSP to the system's gain stability budget. The upper limit on the accuracy, 0.035dB, is derived from SYS4601, which calls for an antenna gain stability dG/G < 0.004.

An additional goal of CSP0061 aims at enforcing time-controlled configurations of the system. Any configuration change in the gain of the CSP must occur at known instants, as commanded by the Monitor & Control subsystem. More requirements may be added to this section in the future as needed.

8.1.2.2 Timing requirements

System requirements SYS2002 and SYS2003 call for ngVLA data products that can be retroactively time referenced to a global time standard such as GPS, TAI or UTC. This is attained by referencing data products with respect to a locally generated central time reference. The resulting timestamps are retroactively corrected offline using the time difference between the central time standard and the global one.

The DBE is responsible for generating timestamped data referenced to the locally generated antenna time reference. Upon reaching the CSP, these timestamps undergo regeneration based on an externally provided delay model. This process ensures that subband data streams are referenced to the central time standard and aligned in time before undergoing beamforming or cross-correlation. The SBP achieves this through the application of phase-delay models provided by the CSS (refer to Assumption [10\)](#page-16-4). All data products produced by the CSP must be timestamped using the central time standard.

Since the timestamping process on the CSP depends on external sources (antenna time reference input, phase-delay models, etc.) the intent of CSP0060 is to specify the maximum error contribution from the CSP to the system timing error referred to by SYS2002 and SYS2003.

The value of 10 ps is based on the timing error budget for the ngVLA system specified by [\[AD10\]](#page-6-15). When determining this value, the DBE was considered as the principal source of error, and the contribution of other CSP systems negligible in comparison. 10 ps equals 1% of the overall system timing precision goal, 1 ns.

CSP0060 requires that the CSP internally corrects significant enough systematic errors as part of its timestamping process. However, a different approach in which systematic errors are corrected by the CSS could be considered in the future if deemed beneficial.

8.1.3 Subarray Operation Requirements

The CSP is required to fully support the operation of the ngVLA as separate subarrays, as defined in Section [3,](#page-8-0) treating each subarray akin to a distinct telescope in its functionality.

Any antenna can be assigned to any subarray to prevent the formation of clusters of antennas assigned together.

The analysis of current system requirements does not anticipate the need to operate more than 10 subarrays at any given time.

The configuration of any subarray should be independent and not influenced by the operation or configuration of any other subarray. As defined, a subarray is expected to have its own dedicated set of processing resources, ensuring the requested independence. Additionally, subarrays must be allocated mutually exclusive subsets of antennas, meaning there should be no overlap in antenna usage between subarrays.

The preceding set of requirements delineates the minimum specifications for subarray operation, providing foundational guidance for the design of the CSP. The subsequent requirements aim to explicate particular facets of the minimum essential capabilities required for the seamless operation of the CSP.

CSP0020 is direct consequence from System Requirements [\[AD03\]](#page-6-12). In this regard, System Requirements clarify that "[…] the addition or subtraction of array elements from a subarray needn't be immediate, and can occur at a natural boundary point such as a scan boundary."

The primary purpose of this requirement is to allow for maintenance of certain antennas without interrupting ongoing observations. However, the current formulation of CSP0020 does not accurately capture this intent; it is excessively strict and may not be feasible in all scenarios. Consequently, a systemlevel revision of this requirement is currently underway.

CSP0058 originated from implementation-related limitations, introducing an artificial distinction between 'primary' and 'secondary' subarrays, with the latter having certain configuration restrictions imposed by the former. This requirement has been withdrawn and may be formally retired in future releases.

Parameter	Req.#	Value	Traceability
Simultaneous	CSP0018	The CSP shall support subarray operation with	SYS0604
Subarray		combinations and capabilities equal to or greater than	SYS0605
Capabilities		the functionality described in Table 1.	

Table 1 – Required sub-array commensality (taken from System Requirements [\[AD03\]](#page-6-12)). The primary or fullfeatured mode is the Y-axis, with the impact on the secondary mode denoted in each column

Table 1 Notes:

- ∗ 'Functional mode' refers to its system-level definition. Mapping of 'system functional modes' to 'CSP functional modes' is design-dependent, and therefore no specifications in this regard are provided in this document.
- 1. Full capabilities in all functional modes must be maintained within the constraints of the maximum data input to the correlator back-end.
- 2. Minimum functionality must include full-bandwidth correlation in one subarray, concurrent with phased array operations in another subarray. Phased array timing, search, and VLBI mode capabilities may have a restricted number of beams or bandwidth to comply with the maximum data input constraint to the correlator back-end.
- 3. Full capabilities in the phased array timing, search, and VLBI modes must be ensured, with interferometric, total power, or on-the-fly mode capabilities (processed bandwidth, time, and/or spectral resolution) constrained by the maximum data input to the correlator back-end.
- 4. Data rates for these functional modes are expected to be sufficiently small to support full capabilities in all functional modes.

CSP0018 serves as the primary requirement guiding the availability of CSP resources for additional simultaneous subarrays necessary to initiate an observation. In CSP designs that allocate resources on a per-subarray basis, the overall size of the CSP is likely dictated by the worst-case scenario of the fullbandwidth whole array. However, CSP designs that allocate resources to subarrays without considering their size must ensure that the minimum capabilities described by CSP0018 are satisfied.

8.1.4 Interferometric Requirements

The following requirements aim at defining the required performance of the CSP for subarrays observing in interferometric mode.

Processing all the available bandwidth shall be allowed in interferometric mode.

CSP0011 allows the CSP to operate in coarser frequency resolutions as a function of the overall bandwidth so that the resulting number of channels does not exceed the specified value. The highest spectral resolution is specified below depending on the Operating Mode.

It is worth noting that CSP0011 does not apply to beamforming modes. This is because the number of frequency channels in a beamformer is determined solely by bandwidth and frequency resolution. On the other hand, adhering to the finest frequency resolution specified in interferometric mode by CSP0022 would lead to an excessively large number of frequency channels spanning the entire bandwidth. CSP0011 provides CSP designers with the opportunity to evaluate scenarios where sacrificing processed bandwidth in favor of finer spectral resolution, such as employing spectral zoom techniques, could offer significant benefits.

The frequency resolution in interferometric mode must be configurable. Otherwise, at least 14 million frequency channels must be supported to meet the required interferometric bandwidth of 14 GHz specified in CSP0021, and the highest frequency resolution of 1 kHz specified in CSP0024.

Note that the subarray independence requirement CSP0019 implies that frequency resolution can be configured independently for each subarray.

The call for independent subband frequency resolution originates from the need for accommodating spectral line and continuum observations in a single setting, as described in System Requirements [\[AD03\]](#page-6-12).

CSP0062 serves as the initial effort to guide CSP designers regarding the flexibility in establishing the required frequency resolution. Higher-level requirements do not explicitly provide any indication in this

regard. Nevertheless, it is evident that the standard operation mode does not involve the highest frequency resolution, as it leads to an impractical number of frequency channels. Additionally, not every value can be employed as a valid frequency resolution configuration. A minimum requirement of one octave has been considered reasonable, although further confirmation is needed to validate such granularity.

It is expected that the finest frequency resolutions can only be achieved if at least one other parameter affecting the CSP output data rate is constrained to keep the output data rate within the limits specified by CSP1036. This means that either the number of antennas in the subarray, the bandwidth, or the time resolution must be constrained with respect to the maximum CSP capabilities to control the CSP output data rate.

The goal of reaching integration times of 1ms in CSP0024 refers to the minimum time resolution, not the quantization step of the configurable time resolutions. Using a logarithmic set of values as the configurable time resolutions may be acceptable, e.g., [100ms, 200ms, 400ms, ...]. There is no clear indication in higherlevel requirements what set of values would be acceptable. OTF modes have been included within the supported range, as the scan mode makes no qualitative difference in the CSP operation. The data rate at the CBE input may impose limitations on the total bandwidth observable at the shortest integration times. Configurations requiring per-baseline integration times will be accommodated by the CSS. Additionally, it is important to note that the coarsest time resolution specified in SYS2001, 5 seconds, pertains to the final data product rather than the CSP output. There is a possibility that this value could be decreased in the future through long-term visibility integration at the CSS.

Channel passband flatness will be determined by correlation loss requirements. The specific requirement will be developed at the SBP level, where the fine frequency channelizer resides.

The frequency response of the CSP within the band of a frequency channel produces a correlation or SNR loss with respect to an ideal rectangular function. The effect of slope, ripple, etc., can be computed according to formulas described [\[RD04,](#page-7-8) [RD05\]](#page-7-9). For example, for a correlation loss of 0.05%, the maximum sinusoidal peak-to-peak ripple in an otherwise perfectly rectangular channel should be less than 0.39 dB.

The frequency selectivity specified in interferometric mode satisfies the System emissive dynamic range requirement SYS6106. It also satisfies the absorptive dynamic range SYS6105 assuming a certain decreasing trend of the sidelobe level. Quantization of the window coefficients must also be considered as it could limit the sidelobe decay.

CSP0026 is likely more than what is necessary to fulfill SYS6105 or SYS6106 (spectral dynamic range requirements). Instead, it has been deemed a reasonable assumption of CSP capabilities.

In practice, the CSP may compute all four polarization correlation products, but must be able to select which ones are output for better control of the output data rate.

CSP0067 currently serves as a placeholder for future requirements pending coordination of the synchronization method at a system level. Given that data at the correlator input has been referenced to central time, it is conceivable that the CSP may need to synchronize integration intervals of the autocorrelation products with externally provided parameters to fulfill the requirements of CSP0067.

8.1.5 Beamforming Requirements

The following requirements define functional and performance capabilities of the beamforming operating mode.

CSP0028 is specified for the minimum aperture of the Main Array as defined in SYS1301. It is understood that the intent is to support beamforming capabilities for the true final configuration of the Main Array, which likely will increase the aperture.

When provided with the proper beamforming and polarization calibration coefficients, the beamformed radiation pattern can meet polarization dynamic range requirements, include nulling directions, and control its side-lobe level, as per System Requirements [\[AD03\]](#page-6-12). Therefore, the responsibility of such capabilities lies in the subsystem generating those coefficients.

As per System Requirements [\[AD03\]](#page-6-12): "The need for phased array capability over the full main array is due to the expected sub-array allocations. […] The use of the main array aperture size in this definition is not intended to preclude using the extended baselines […] so long as the phased sub-array does not exceed 700 km in extent."

The number of beams is for the whole array. Hence, it might be distributed over subarrays in this operating mode. CSP0029 accounts for the most demanding use case, currently specified by SYS0203 (Phased Array Operating Mode requirements). SYS0301 (Pulsar Timing Operating Mode requirements), SYS0401 (Transient and Pulsar Search Operating Mode requirements), and SYS0501 (VLBI Operating Mode requirements) demand less or equal capabilities.

In practice, the CSP designs under consideration can exchange bandwidth for the number of beams. CSP0029 specifies the minimum number of beams for the full bandwidth specified in CSP0030.

The minimum bandwidth of the beamformer has been determined as the best value solution to inform the designer about minimum requirements that must be satisfied for subarray operations (in which some other subarrays may be simultaneously observing using different functional modes) along with other requirements, particularly the number of beams in CSP0029. A particular CSP design might support increased bandwidth for the beamformer if deemed advantageous or achieved at a relatively low cost. Similarly, some CSP designs might allow different trade-offs to increase the per-beam bandwidth, such as allocating more bandwidth for fewer beams.

While the SBA employs smaller antennas, resulting in a wider field of view, the much larger aperture size when beamforming the main array means that the requirements are more stringent. Nonetheless, explicitly mentioning the SBA aims to clarify that there are no restrictions on the beamformer's field of view for the SBA.

The beamformer's field of view, aperture, and correlation loss requirements could guide the designer in selecting the most advantageous beamforming technique, such as True Time Delay beamforming or a narrowband approximation based on Phase-Shift beamforming.

Polarization correction is expected to happen at the same time as the application of beamforming complex coefficients.

Concurrent visibilities required by CSP0034 are required for calibration purposes. It is expected that the synthetic beam for which visibilities are measured is pointed toward a calibrator within the primary beam of the antenna.

The CSP is required to adhere to CSP0034 while ensuring the fulfillment of simultaneous subarray capabilities as specified in CSP0018. In other words, if additional CSP resources are allocated to meet the requirements of CSP0034, it should not affect the resources available for concurrent observing subarrays.

Compatibility with a standard VLBI format, such as VDIF, is anticipated. This requirement is driven by the expectation of utilizing existing VLBI recording hardware for a potential future scenario where a VLBA recorder could be connected to the CSP as a custom back end.

8.1.6 Pulsar Timing and Search Requirements

The following requirements define the performance and functional requirements of the Pulsar Timing and the Search operating modes of the CSP. The associated functions are performed at the PSE, which will usually operate on the beamformed outputs of the SBP.

The above requirements specify general processing capabilities in Pulsar Timing and Search observing modes.

The objective is for the PSE to be capable of processing the complete output from the beamformer. It is important to note that the current design permits the adjustment of the trade-off between the number of beams and the bandwidth allocated per beam. This means that fewer beams can be produced with an increased bandwidth per beam.

Note that CSP0039 permits halving the processed beam-bandwidth product when the functional mode involves dedispersion and folding. In essence, the PSE design should be scalable, allowing for the upgrading of processing capabilities in the future without necessitating the retirement of existing hardware.

The minimum time resolution has been determined by the requirement to produce 2048 "bins" assuming a 1-ms pulse profile, surpassing the necessary resolution for transient and pulsar searches. To handle the

data rate effectively, it is recommended to adjust and potentially increase the time resolution. For example, a time resolution of 14 ms aligns with generating 2048 bins within a 30-second pulse. Refer to CSP0055 for an additional requirement concerning the number of bins.

The relationship between time and frequency resolutions is interdependent. Data that is finely frequencychannelized will naturally result in poorer time resolution. The product of both resolutions will consistently exceed a value greater than one, meaning that the PSE will not support oversampling.

The SNR loss specified above is distinct and supplementary to other SNR losses outlined, particularly the beamforming SNR loss (CSP0032). In both the Pulsar Timing and Search Modes, the CSP initially synthesizes a signal through beamforming, followed by specific processing tailored to the operating mode. CSP0042 and CSP0068 pertain solely to this specialized processing.

8.1.7 RFI Mitigation Requirements

CSP0049 is a placeholder of proper future RFI detection and excision requirements specifying minimum performance requirements.^{[2](#page-32-3)} The most recent assessment of the needs of the ngVLA in terms of RFI handling can be found in [\[RD12\]](#page-7-10). The analysis therein points out that the necessity for RFI mitigation algorithms within the CSP must be determined through an evaluation of their effectiveness and a comprehensive characterization of the ngVLA radio environment.

8.1.8 Delay and Phase Tracking Requirements

The requirements in this section apply to both interferometric and beamforming modes. The update rate is determined by interferometric mode requirements.

 2 RFI mitigation requirements shall be fully developed by PDR.

For context, the maximum geometric delay in 10,000-km baselines is 3.3 ms, which is small compared to the expected network latency (more details in the specific interface requirements below). However, the geometric delay compensation requirement applies to the main phase center position. Multiple phase centers will require differential delay corrections and are fully supported (i.e., anywhere within the same antenna lobe) only for the beamforming-specific aperture limit; see CSP0028.

It is assumed that the phase and delay correction model parameters are computed by the CSS. Therefore, requirements such as SYS0602 (array phase center preservation) or the location of the array phase center have no impact on CSP requirements.

The delay and phase tracking update rate specified in CSP0051 does not refer to the rate at which the CSP receives new delay and phase models from the CSS, as this can be much slower. Additionally, it does not refer to the rate at which fine delay corrections are internally updated within the CSP, which needs to be much faster. Instead, the intent of CSP0051 is to specify the update rate required for the delay model during On-The-Fly (OTF) mapping, ensuring that the phase center accurately follows the antenna's movement across the sky. This requirement is still under development, pending the finalization of the CSS and CSP interface, as well as the delay model management strategy.

The current design includes support for Sampler Clock Offset compensation. The adoption of this technique is driven by the desire to enhance the mitigation of self-generated RFI at the digitizer, as well as to address spectral components that may be aliased during the digitization process.

CSP0053 is somewhat redundant with CSP0009 and is included here only to emphasize that the SNR loss of the tracking algorithm must be accounted for in the overall CSP budget. It is up to the designer to

determine the distribution of the overall CSP allocation across different DSP stages, including delay and phase tracking.

It has been determined that OTF mapping requirements do not impose any additional demands on the CSP, other than the delay model update rate requirements specified in CSP0051.

8.1.9 Dedispersion Requirements

This value is intended for dedispersing pulses originating from hypothetical observations of pulsars near the center of the Milky Way.

8.1.10 Folding Requirements

The above set of requirements were extracted from [\[RD03\]](#page-7-7).

8.1.11 Legacy DBE Requirements

The following set of legacy requirements was included at a time when the functional partition of the DBE and the CSP was unclear. These requirements specifically apply to the DBE and are retained here solely for traceability purposes; however, they may be removed in future releases.

8.1.11.1 Sideband Separation Requirements

8.1.11.2 Subband Generation Requirements

8.2 Interface Requirements

In this section, requirements are derived from the applicable ICDs as listed in Section [2.2.](#page-6-2) As stated in the SEMP [\[AD01\]](#page-6-4), ICDs define the interface, but do not contain any requirements. All interface requirements that drive the design and verification of the subsystem shall be listed in this section.

Currently, most of the interface requirements are simple placeholders that will be fully developed during the PDR phase of the project.

All requirements related to DBE interfaces have been withdrawn but are still shown herein for documentation purposes.

8.2.1 020.10.40.05.00-0095 ngVLA Site Buildings Interface Requirements

The ngVLA Site Buildings subsystem (NSB, CI number 020.61.10.00.00) hosts all CSP elements in a central facility, the Central Electronics Building (CBE), that provides an environmentally controlled space, power, and RFI shielding. This interface defines the CSP dimensions, thermal load, EMI emissions, and fixing.

These ranges are generally supported by commercial electronic components. Subsystem requirements are defined in Section [8.](#page-18-4)

CSP1028 is a placeholder for a future requirement. The current assumption is that the CSP equipment complies with applicable commercial regulations, while the RFI shielding provided by NSB guarantees no significant degradation of the system sensitivity. This requirement will be determined from the ICD specification.

CSP1050 includes all equipment comprising the CSP. For example, it would include the coolant distribution units of a liquid cooling system used by the CSP, but not the HVAC equipment used for room temperature control. The current value of 2MW was derived from the reference design and has been significantly reduced in the current design concept [\[RD01\]](#page-7-5).

8.2.2 020.10.40.05.00-0105 CSP–MCL System Interface Requirements

This interface aims to support the M&C data interface between the CSP at the central facility and the M&C subsystem (MCL, CI number 020.50.25.00.00). It defines the extent and cadence of monitor data, as well as configuration parameters and operational commands. It also specifies the communication protocols and the physical and mechanical interface between the CSP and MCL.

8.2.2.1 Configuration Parameters

The CSP receives its observation configuration parameters via the MCL-CSP interface. These parameters are then processed by the CMC, which converts them into low-level commands as necessary to control the hardware.

A number of these configuration parameters are initially received at the beginning of a scan and persist unchanged throughout its duration, necessitating no updates during this period. Nonetheless, there exist specific configuration parameters that mandate periodic updates throughout the scan. The subsequent set of requirements is established to outline the essential minimum capabilities of the CSP to effectively process and implement the streamed parameter updates.

The following is a preliminary description of the parameters that the CSP needs to process. The processing time indicates the duration required for the CSP to process and implement the received configuration. Configuration parameters received with an anticipation shorter than the processing time will be applied as soon as possible, which may occur after their designated applicability time. The CSP is responsible for communicating such an event and flagging any data products that may be affected. Specific procedures to address this potential issue will be developed in [\[AD22\]](#page-6-10).

Table 2 – Configuration parameters of the CSP received from the MCL subsystem.

³ The system assumes continuous updating of the phase reference position during on-the-fly (OTF) observing modes. System Requirements [\[AD03\]](#page-6-12) mandate a minimum update frequency of 10 Hz for the phase reference position, with a target of achieving 20 Hz.

The CSP must not assume that updates will be received at any specific cadence, including the indicated cadence or any other. The above requirement assigns full responsibility to the MCL system for ensuring the proper update of configuration parameters.

8.2.3 020.10.40.05.00-0114 CSP– Online Data Acquisition Interface Requirements

This interface supports the transmission of data and metadata generated by the CSP to the Computing and Software System (CSS, CI number 020.50.00.00.00), particularly the Online Data Acquisition subsystem (ONL, CI number 020.50.10.00.00) [\[AD23\]](#page-6-9). The CSS is responsible for further processing the data as needed for calibration and archiving. This interface describes both the physical and logical specifications.

8.2.4 020.10.40.05.00-0119 CSP–Central Fiber Infrastructure Interface Requirements

The elements of the CSP at a central facility receive data from the antennas via the Central Fiber Optic Distribution subsystem (FIB, CI number 020.55.20.00.00). This interface is expected to use industry standards allowing high data rate (>100 Gb/s per link), long distance (~100 km) communications. The CSP must account for common operational capabilities of such systems. This interface aims at defining the physical specifications, but the logical specification belongs to a separate interface between the DBE and the SBP. Note that this interface must also cover the physical specification between the FIB subsystem and the DBE in cases where the latter is located at the central facility (could be the case for the SBA).

The System Requirements' goal of connecting to other flagship capabilities states, "A minimum capability would provide the requisite delay buffers to accommodate the projected network delays to the GBT. A more capable implementation would have delay buffers to interface with Effelsberg and phased ALMA." Specific network latency required is still under assessment.

It is anticipated that the communication links from the antennas may incur data loss, particularly in longdistance links using third-party infrastructure. The CSP shall be tolerant of this data loss, meaning that it must be integrated into operation, by monitoring and reporting such events as will be determined in the future. CSP performance, however, will be impacted by data loss.

Note that the current parameter of 250 ms has been determined as a trade-off value between memory resources required at the CSP and the expected network latency when transmitting several hundred gigabits per second through commercial fiber from the outermost antennas. The uncertainty surrounding this requirement at the time of writing is significant, and this value may change in the future.

8.2.5 Legacy CSP–LO Reference & Timing Generation Interface Requirements

Many interface requirements are specific to a particular design. In the current CSP design concept, the CSP operates asynchronously with respect to ngVLA central time, eliminating the need for a frequency reference. Additionally, CSP time is solely utilized to determine when computations are performed or, equivalently, when data flows through the system. Therefore, only a coarse notion of central time within millisecond precision is necessary for the CSP, and this can be more cost-effectively achieved by leveraging an existing interface (CSP-MCL), rather than implementing an additional interface for time distribution. This may be based, for example, on the Precision Time Protocol. Consequently, there is currently no interface between the CSP and the RTG subsystem, and the related set of requirements has been withdrawn.

This set of requirements is kept herein for legacy purposes only and may be removed in future releases.

8.2.6 Legacy DBE Interface Requirements

The following requirements have been withdrawn as they are related to interfaces of the DBE other than the DBE-CSP interface. Traceability of related DBE retirements point now to the proper ICD.

8.3 Safety and Security Requirements

This section defines all design requirements necessary to support the Level-1 Safety, Security and Cybersecurity requirements derived from [\[AD03\]](#page-6-12), [\[AD07\]](#page-6-16), and [\[AD08\]](#page-6-17).

The above set of requirements serve as placeholders and will be developed in the future.

8.4 Reliability, Availability, and Maintainability Requirements

This section defines all RAM requirements and Logistic Support requirements derived from [\[AD03\]](#page-6-12).

CSP3018 is not aimed at scientific data but fast read out of monitor points. See [\[RD09\]](#page-7-11) for further context.

The intent of CSP3021 is to require that preventive maintenance be done on a reduced number of LRUs, which can be taken out of operation during maintenance, while the rest of the CSP equipment remains operational. Additional sub-elements (e.g., SBP Units) may be installed as needed to guarantee minimum operational capabilities during maintenance.

CSP3023 applied only to the DBE and has been withdrawn from the set of CSP requirements.

CSP3020 pertains to critical failures that render the CSP inoperable. However, individual node failures affecting antennas or bandwidth, which lead to a graceful degradation of CSP processing capabilities, will necessitate distinct considerations.

8.5 Configuration and Document Management Requirements

This section defines Configuration Management requirements and Documentation requirements, derived from [\[AD03\]](#page-6-12).

8.6 Life Cycle Requirements

This section defines the System Life Cycle requirements, including design and development, AIV, and CSV as derived from [\[](#page-6-3)[AD03\]](#page-6-12).

In System Requirements [\[AD03\]](#page-6-12), operational life is defined to start at the full operations milestone and close-out of the construction project, and SYS2801 sets a duration of 20 years. However, the operational life of the CSP is defined to start with construction and commissioning activities, 10 years ahead of full operations.

Critical spares are defined as parts that are likely to be obsoleted over the operating life, are unlikely to have market substitutes, and cannot be produced/ordered in small volumes.

The motivation to call for a virtual machine is to ensure compatibility and usability of the compilation chain over the life of the facility.

CSP5011 functions as a provisional framework for anticipated future needs. The goal is to implement consistent design standards and practices throughout the telescope. However, given the extensive use of Commercial Off-The-Shelf (COTS) systems and outsourcing by the CSP, strict adherence to these standards may result in an unjustified rise in costs. Consequently, CSP5011 and its associated requirements are subject to revision as a goal, rather than requirement.

9 Key Performance Parameters (KPPs)

Key Performance Parameters (KPPs) identify critical subsystem capabilities or characteristics that may either have a detrimental impact on the effectiveness of efficiency of the system if not met, or could have a very large positive impact if the specification is exceeded. Subsystem KPPs typically support System KPPs and there should be traceability between them. Each KPP must have a threshold range and objective value. The responsible engineer designs the subsystem to meet the objective value, but performance within the threshold range is considered acceptable. During the design phase, there should be a concerted effort to optimize the KPPs. If the responsible engineer finds that the minimum threshold level of a KPP cannot be achieved the project office shall be notified immediately.

Full subarray independence is critical for ngVLA operations.

Any limitation to the processed bandwidth should be informed to upper management.

The current design concept allocates 0.6% correlation to the CSP, while the remaining 0.4% is assigned to the DBE. CSP0009 specifies the joint loss, so this KPP must be jointly monitored.

This KPP has a direct impact on the system's sensitivity in Phased Array Operating Mode.

This KPP has a direct impact on the system's sensitivity in Pulsar Timing and Search Operating Modes.

The timestamping accuracy of the CSP is deemed negligible when compared to the timing error budget of the ngVLA system. Any deviation from this assumption may impact the system's ability to meet dynamic range requirements, among other potential adverse effects.

Many CSP requirements are critical in the sense that the System relies solely on the CSP to satisfy a requirement. Therefore, if not met, they would have a significant impact on the system's effectiveness. Nevertheless, they have not been included as KPP as their satisfaction is not deemed at risk, and they do not support any system KPP. Future revisions may include additional KPPs based on updated risk assessment.

10 Verification

The design will be verified to meet the requirements by analysis (A), inspection (I), demonstration (D), or test (T), each defined below.

Verification by Analysis: The compliance of the subsystem to the requirement is demonstrated by appropriate analysis (hand calculations, finite element analysis, modeling and simulation, etc.).

Verification by Inspection: The compliance of the subsystem to the requirement is determined by a simple inspection of the subsystem or of its design documentation.

Verification by Demonstration: The compliance of the subsystem to the requirement is determined by a demonstration.

Verification by Test: The compliance of the subsystem to the requirement is determined by means of a test with and associated analysis of test data.

Multiple verification methods are allowed over the course of the design phase. The primary (final) verification method to be used for the product during the qualification phase prior to its Critical Design Review is identified below.

10.1 Verification Methods

10.1.1 Functional and Performance Requirements

10.1.2 Interface Requirements

10.1.3 Safety and Security Requirements

10.1.4 Reliability, Availability, and Maintainability Requirements

10.1.5 Configuration and Document Management Requirements

10.1.6 Life Cycle Requirements

10.1.7 Environmental Requirements

10.2 Verification Requirements

Table 3 – Set of use cases used for verification of Correlation Loss requirement CSP0009. More use cases may be added in future releases of this document.

11 Appendix

11.1 Abbreviations and Acronyms

020.40.00.00.00-0001_REQ_CSP_REQUIREM **ENTS**

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