Digital Backend/Data Transmission System: Technical Requirements

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1 Introduction

1.1 Purpose

This document presents a set of technical requirements for the design of the ngVLA Digital Backend/Data Transmission System (DBE/DTS) work package. Many requirements flow down from the preliminary ngVLA System Requirements [AD02], which in turn flow down from the preliminary ngVLA Science Requirements [AD01].

The science goals are presently being elaborated by the Science Advisory Council (SAC) and Science Working Groups (SWGs), and are captured in a series of draft use cases. This document reflects preliminary analysis of these use cases and the flow down recursively to the science, system and subsystem requirements.

1.2 Scope

The scope of this document is the ngVLA DBE/DTS work package. This describes an opto-electronics system that receives unformatted data streams from the Integrated Downconverter/Digitizer Subsystem, performs substantial processing and data reduction on them, then formats and modulates them onto optical carriers for transmission to the Array Center via private and/or commercial fiber optic infrastructure.

This requirements document establishes the performance, functional, design, and test requirements applicable to the ngVLA DBE/DTS work package. It also includes interface requirements that must be defined.

2 Related Documents and Drawings

2.1 Applicable Documents

The following documents are applicable to this Technical Specification to the extent specified. In the event of conflict between the documents referenced herein and the content of this Technical Specification, the content of this Technical Specification shall be considered as a superseding requirement.

Reference No.	Document Title	Rev/Doc. No.
AD01	Science Requirements	020.10.15.00.00-0001-REQ
AD02	Preliminary System Requirements	020.10.15.10.00-0003-REQ
AD03	Operations Concept	020.10.05.00.00-0002-PLA
AD04	Protection Against Electric Shock – Common Aspects for Installation and Equipment	IEC 61140:2016
AD07	Insulation Coordination for Equipment within Low-Voltage Systems	IEC 60664
AD08	Occupational Safety and Health Standards for General Industry	29 CFR Part 1910
AD10	Military Handbook, Reliability Prediction of Electronic Equipment	MIL-HDBK-217F
AD11	Non-Electronic Parts Reliability Data	NPRD-95
AD12	Electromagnetic Compatibility	IEC 61000-3-5
AD13	Integrated Downconverters and Digitizers Design	020.30.15.00.00-0002-DSN
AD14	ngVLA Memo 29: An Integrated Receiver Concept for the ngVLA	ngVLA Memo 29
AD15	System Requirements	020.10.15.10.00-0003-REQ
AD16	System Environmental Specifications	020.10.15.10.00-0001-SPE
AD17	System EMC and RFI Mitigation Requirements	020.10.15.10.00-0002-REQ
AD18	System-Level Electrical Requirements	020.10.15.10.00-0005-REQ
AD19	System-Level Mechanical Requirements	020.10.15.10.00-0006-REQ

2.2 Reference Documents

The following references provide supporting context:

Reference No.	Document Title	Rev/Doc. No.
RD01	Subsystem Reference Design Description: Digital Back End/Data Transmission System	020.30.25.00-0002-DSN

3 Overview of DBE/DTS Technical Requirements

3.1 Document Outline

This document presents the technical requirements of the ngVLA DBE/DTS work package. These parameters determine the overall form and performance of the DBE/DTS work package.

The functional and performance requirements, along with detailed explanatory notes, are found in Section 4. The notes elaborate on the meaning, intent, and scope of the requirements. These notes form an important part of the definition of the requirements and should guide the verification procedures. In many cases the notes contain an explanation or an analysis of how the numeric values of requirements were derived. Where numbers are not well substantiated, this is also documented in the notes. In this way, the required analysis and trade-space available is apparent to scientists and engineers who will guide the evolution of the ngVLA DBE/DTS work package concept.

Requirements pertinent to interfacing systems are described in Section 5. Initial requirements are noted by interface, along with identified parameters for Interface Control Documents (ICDs) that will fully define the interfaces as the design progresses. Safety requirements applicable to both the design phase and the functional DBE/DTS work package are described in Section 7. Additional requirements for the design phase are described in Section 8. Documentation requirements for both technical design documentation and software are provided in Section 9. Requirements for the Verification and Test, from the conceptual design through to prototype, are described in Section 10.

3.2 Project Background

The Next Generation Very Large Array (ngVLA) is a project of the National Radio Astronomy Observatory (NRAO) to design and build an astronomical observatory that will operate at centimeter wavelengths (25 to 0.26 centimeters, corresponding to a frequency range extending from 1.2 GHz to 116 GHz). The ngVLA will be a synthesis radio telescope composed of approximately 244 reflector antennas each of 18 meters diameter, and 19 reflector antennas each of 6 meters diameter, operating in a phased or interferometric mode.

The array's signal processing center will be located at the Very Large Array site on the Plains of San Agustin, New Mexico. The array will include stations in other locations throughout New Mexico, west Texas, eastern Arizona, and northern Mexico. Long baseline stations are located in Hawaii, Washington, California, Iowa, Massachusetts, New Hampshire, Puerto Rico, the US Virgin Islands, and Canada. Operations will be conducted from both the VLA Control Building and the Array Operations Center in Socorro, NM.

3.3 General DBE/DTS Work Package Description

This work package leads to the design of a Digital Back End/Data Transmission System Subsystem that receives data from the Integrated Downconverter/Digitizer subsystem, performs the primary digital processing required at the antenna, and prepares data for transmission across private and public telecommunications infrastructure. This subsystem is concentrated in a single, highly integrated RFI shielded module located in the pedestal area of each ngVLA antenna.

Digital data streams produced in the Integrated Downconverter/Digitizer (IRD) Modules located in the Front End (FE) are received in the DBE/DTS module via 13 single-mode fibers. Clock recovery and de-serialization is performed on the data which is then fed to digital processing blocks where functions such as channelization, digital downconversion, re-quantization, RFI tagging or excision, etc. can be performed.

Processed data is then formatted into standard telecommunication formats (i.e. Ethernet, SONET) and placed back into the optical domain for transmission over private or commercial fiber-optic networks.

3.4 Summary of DBE/DTS Work Package Requirements

The following table provides a summary of the major requirements in order to provide the reader with a high-level view of the desired system. Should there be a conflict between the requirements listed here and the descriptions in Sections 4 through 10, the latter shall take precedence.

3.4.1 General Functional Specifications

Parameter	Summary of Requirement	Reference Reqs.
Single Channel Input Data Rate	56,000 Mbps (on each optical carrier from IRD)	IRD0711-716 IRD0721-726
Number of Input Channels	46 (4 each from Bands 2–6 IRD modules, 2 from Band 1 IRD module)	IRD0711-716 IRD0721-726
Input Data Sample Rate/Bit Depth	7×10^9 8-bit samples/sec or 14×10^9 4-bit samples/sec	IRD0711-716 IRD0721-726
Input Data Format	Unformatted raw data	IRD0711-716 IRD0721-726

4 DBE/DTS Functional and Performance Requirements

These requirements apply to a properly functioning system under normal operating environmental conditions unless otherwise stated.

4.1 Functional Requirements

Parameter	Req. #	Value	Traceability
Clock Recovery	DBE001	The DBE shall perform clock recovery on the unformatted data streams received from the IRD modules as described in [AD13] and [AD14].	
Coarse Sideband Separation	DBE002	The DBE must perform coarse sideband separation into upper and lower sidebands using the IQ pairs received from the IRD modules as described in [AD13] and [AD14].	
Digital LO for Mixer	DBE003	The DBE must generate a LO for the sub-band selection digital mixer and track and control its phase.	
Sub-Band Selection	DBE004	Using a digital mixer and digitally generated LO, the DBE must be able to tune and select multiple sub-bands.	
RFI Flagging	DBE005	The DBE must be capable of identifying and flagging data in the presence of known or suspected radio frequency interference; details TBD.	
RFI Excision	DBE006	The DBE should be capable of performing digital signal processing to excise certain destructive radio frequency interference from the data stream using specially designed excision algorithms; details TBD.	
Oversampling Polyphaser Filter	DBE007	The DBE polyphaser filters must have an oversampling capability to eliminate concerns with dead zones between sub-bands.	
Apply Timestamp	DBE008	The DBE must apply a timestamp based on the reference clock and timing inputs to data before transmission to the central signal processor.	
Data Encoding	DBE009	The DBE must encode data into format(s) compatible with the data transmission medium being used. This mainly refers to antennas connected to commercial networks.	
Data Transmission	DBE010	The DBE must output optical data streams that can be placed directly on fiber to the array center or is compatible with COTS data transmission equipment at the site.	

4.2 Performance Requirements

Parameter	Req. #	Value	Traceability
Upper/Lower Sideband Isolation	DBE200	>43 dB	
Timestamp Jitter	DBE201	6.4 ns	

4.3 I/O Requirements

Parameter	Req. #	Value	Traceability
Input Data Sample Rate/Bit Depth	DBE103	$7x10^9$ 8-bit samples/sec or $14x10^9$ 4-bit samples/sec	IRD0711-716 IRD0721-726

4.4 Spurious Signals/Radio Frequency Interference Generation

Parameter	Req. #	Value	Traceability
Enclosure RFI Shielding @100 MHz	DBE114	Max EIRP Emission –126 dBm	EMC3010, SYS2104
Enclosure RFI Shielding @1 GHz	DBE115	Max EIRP Emission –126 dBm	EMC3010, SYS2104
Enclosure RFI Shielding @10 GHz	DBE116	Max EIRP Emission –102 dBm	EMC3010, SYS2104

4.5 Environmental Conditions

4.5.1 Normal Operating Conditions

Parameter	Req. #	Value	Traceability
Operating Temperature Range	DBE112	–15 to +35°C	ENV0323
Altitude, etc.	DBE119	2500 meters	ENV0351

4.5.2 Specific Environmental Requirements

Parameter	Req. #	Value	Traceability
Storage Temperature Range	DBE113	–20 to +70°C	020.10.15.10.00-0001-SPE System-Level Environmental Specifications

4.6 Maintenance and Reliability Requirements

Parameter	Req. #	Value	Traceability
Mean Time Between Failures	DBE120	MTBF ≥ 35,040 hrs.	SYS2402

The maintenance and reliability requirements support high-level requirements that limit the total array operating cost. Monitor points/sensors should be included in the MTBF/MTTR analysis, but sensors and other components that can be reasonably deemed ancillary to operation may be removed from the determination of compliance with the MTBF requirement. "Failure" will be defined as a condition that places the system outside of its performance specifications or into an unsafe state, requiring repair.

4.7 Monitor and Control Requirements

The DBE/DTS work package shall measure, report, and monitor parameters that allow for determination of its status and may help predict or respond to failures.

Parameter	Req. #	Value	Traceability
Input Power Supply Voltage	DBE900	The DBE/DTS module shall measure, report, and monitor the input DC supply voltage to the module.	SYS2701
Input Optical Power Monitor	DBE901	The DBE shall report actual optical power or digital status indicating optical power on all inputs is within an acceptable limit. Subject to power monitoring capability of the optical receiver.	

Parameter	Req. #	Value	Traceability
Input Clock Power	DBE902	The DBE shall report actual power or digital status indicating power on the clock input is within an acceptable limit.	
Input Timing Signal	DBE903	The DBE shall report that a valid timing signal is received at an appropriate level and passes all built-in error checking.	
Module Temperature(s)	DBE904	The DBE shall report actual temperatures of heatsinks, power supply, internal ambient temperatures and the status of any internal over temperature protection circuits.	
Electronic Serial Number	DBE905	The integrated modules shall report a unique electronic identification upon request.	
Standby Mode	DBE906	The DBE shall be capable of entering a low-power standby mode on command. M&C communications shall still be functional in this mode.	
Automatic Initialization	DBE907	The DBE Module shall automatically boot into a nominal operational mode on power-up, absent any command from M&C.	
Data Transmission Link Status	DBE908	The DBE module shall report the connection status of the 100 Gbps Ethernet links used for data transmission.	
Clocking System Status	DBE909	The DBE module shall report the lock/tuning status of any clock generation circuitry in the module. This includes FPGA clocking resources and any external PLL oscillators used in the module.	
Data Quality Sampling	DBE910	The DBE module shall be capable of grabbing a chunk of sampled data from multiple points in the system and of sufficient size to be processed into useful diagnostic data. This could either be passed as raw data or processed locally into formats useful for diagnostics. Results are transmitted via the M&C network.	

The expectation with self-monitoring is that the M&C system will expose lower-level sensors to the M&C system when queried. The cadence of access is flexible, and is not expected at high rates (typical access might be on second to minute scales). Any high-cadence monitoring should generally be internal to the DBE/DTS work package control system with a summary output on the interface.

Other features of the M&C interface are specified in the Monitor and Control ICD. Lifecycle costs include manufacturing, transportation, construction/assembly, operation, and decommissioning.

4.8 Lifecycle Requirements

Parameter	Req. #	Value	Traceability
Design Life	DBE1801	The DBE/DTS work package shall be designed to be operated and supported for a period of 20 years.	SYS2801
Life Cycle Optimization	DBE1802	The DBE/DTS work package design shall minimize its lifecycle cost for 20 years of operation.	SYS2802

5 Interface Requirements

This section provides information about the interfaces of the DBE/DTS work package. Interface Control Documents (ICDs) are required between the DBE/DTS work package and all connecting systems. In many cases, specifications for the interfaces are not yet available, but the broad scope of the ICD can be defined.

These interfaces shall be developed and documented by the DBE/DTS work package designer, and approved by ngVLA, as part of the DBE/DTS work package reference and conceptual design efforts, and updated throughout the design. Post CoDR, the ICD shall only be updated through formal project change control processes.

5.1 Interface to the Integrated Downconverter/Digitizer Subsystem

Data processed by the DBE/DTS subsystem is produced in the 13 integrated downconverter/digitizer (IRD) modules located near the receivers in the antenna. These produce data in one of two formats:

- 8-bit samples at 7 Giga samples per second, or
- 4-bit samples at 14 Giga samples per second.

The data streams are modulated onto optical carriers at 1310 nm. The outputs of these IRD modules are optically combined onto 16 single mode fibers. These fibers enter through 16 terminals of a 36-fiber APC type ruggedized circular connector. Each of these data streams arrives at the DBE/DTS PCBs on a single mode fiber containing an LC type connector that connects to one of the QSFP28 form factor optical transceivers. The optical transceivers achieve 56 Gbps transfer rates using four-level PAM4 modulation.

Signal at Interface	Type	Parameter	Value	Comments
Digital IFs	Input	Data Format Data Content Connector Physical Format Nominal Wavelength Colors/Lanes Baud Rate Effective Bit Rate Modulation # of fibers	Unformatted I/Q or Nyquist QSFP Single-Mode Fiber 1310 nm 4 (2 from Band 1) 28 Gbaud/Lane 56 Gbps/Lane PAM4 13	PAM4 modulation carries 2 bits per symbol, so “effective” 56 Gbps per lane is achieved by transmitting 28 billion symbols per second. Number of fibers: 13 nominal

5.2 Interface to the Reference Signal Subsystem

The DBE/DTS module receives a 156.25 MHz CW clock from the antenna reference subsystem. This signal arrives as a 156.25 MHz CW signal modulated onto a 1310 nm optical carrier. It enters the module on one terminal of a 36-fiber APC type ruggedized circular connector on the front face of the module. The reference fiber is connected to an optical receiver to be converted to an electrical 156.25 MHz clock that feeds all of the FPGAs.

The DBE/DTS module also receives a timecode signal from the antenna reference subsystem. This is a digital timing signal modulated onto a 1310 nm optical carrier. It enters the module on one terminal of a 36-fiber APC type ruggedized circular connector on the front face of the module. The timecode fiber is connected to an optical receiver to be converted to an electrical timecode signal that feeds the FPGAs.

Signal at Interface	Type	Parameter	Value	Comments
Master Clock	Input	Frequency Signal Type Level Connector Phase Noise/Jitter	156.25 MHz Sine Wave (CW) 0 dBm SMA 2.5 ps	 SYS5001
Time Code	Input	Signal Type Format Connector Resolution	Optical/Digital IRIG-A Part of fiber circular connector ≤1ms	 (or similar)

5.3 Interface to the Antenna Structure

5.3.1 Electrical Infrastructure

Electrical power to the DBE/DTS module(s) is a single –48 VDC connection from the –48 VDC power subsystem in the antenna pedestal room. This enters the module through a two-terminal filtered, locking type power connector on the front face of the module. Battery backup is provided through the –48 VDC power subsystem. No addition batteries are used for the DBE/DTS subsystem. The –48 VDC input to the module is over-current protected by a single-use fuse internal to the module. The input connector will be keyed to assure correct polarity, so no reverse polarity protection is required.

Signal at Interface	Type	Parameter	Value	Comments
Main Power	Input	Signal Type Nominal Level Current Connector	DC Voltage –48 Volts DC 10 Amps Max Filtered locking circular connector	020.10.15.10.00-0005-REQ System-Level Electrical Requirements

5.3.2 HVAC

The DBE/DTS module has external heatsink fins on both sides of the enclosure. Forced-air cooling in the rack will move air across these fins. The module is sealed so no air penetrations or air filtering is required. The module is designed with internal thermal protection to shut down or reduce power dissipation in the event of HVAC failure.

5.3.3 RFI Mitigation

The module is RFI shielded to prevent interference with the astronomical signals received by the antenna. Shielding effectiveness is outlined in Section 4.1.

5.4 Interface to the Monitor and Control System

The M&C connection uses Gigabit Ethernet connection to the antenna M&C Ethernet switch. Two fibers (transmit and receive) connect to the module via two terminals of the 36-fiber APC type ruggedized circular connector on the module face. Internally the fibers connect to an SFP+ type transceiver connected to the internal M&C processor.

6 Safety

6.1 General

Parameter	Req. #	Value	Traceability
Weight	DBE121	≤50 lbs	020.10.15.10.00-0006-REQ System-Level Mechanical Requirements

6.2 Safety Design Requirements

6.2.1 Fire Safety

The module will have a sealed metal enclosure with fusing to minimize fire risk in internal electronics or external wiring. Thermal protection will minimize power dissipation in the event of HVAC or internal component failure.

6.2.2 Mechanical Safety

The module weight will be kept below 50 lbs. to minimize the requirement for two-person lift. Secure handles will be provided to enable easy transportation of the module. The enclosure will be designed to minimize sharp edges.

6.2.3 Electrical Safety

Electrical equipment installed on the antenna shall comply with their relevant international or US product standard. Electrical installations and equipment shall be specifically built and/or derated to safely perform their intended functions under the applicable environmental conditions. Insulation shall be coordinated in conformity with IEC 60664 [AD07] while taking into account the altitude of up to 2500 m above sea level.

The –48 VDC will be protected with fuses to protect both internal electronics and external power supply infrastructure from damage in the event of a failure in the module. Reverse polarity protection on the power input is provided by a keyed connector. Switching regulator modules will be implemented with all fuses and noise suppression or safety (X and Y type) film capacitors as recommended by the manufacturer.

6.2.4 Handling, Transport, and Storage Safety

The design of the DBE/DTS work package shall incorporate all means necessary to preclude or limit hazards to personnel and equipment during assembly, disassembly, test, and operation.

7 Design Requirements

7.1 Analyses and Design Requirements

7.1.1 Reliability Availability Maintainability Analysis

A Reliability Availability Maintainability analysis shall be performed to locate weak design points and determine whether the design meets the Maintenance and Reliability requirements. The ngVLA project will apply the Parts Count Method for predicting system reliability as described in MIL-HDBK-217F, but the designer may propose to use other methods. For non-electronic parts, the values of NPRD-95 [AD11] or data from manufacturers or other databases may be used.

Another, but more time-consuming (and considered more accurate) method, the Parts Stress Analysis Prediction, is also described in MIL-HDBK-217F. This may be used if the result of the Parts Count Method does not comply with the Maintenance and Reliability requirements.

The ngVLA equipment will typically operate at 2200 m above sea level, where temperature and pressure might decrease the MTBF relative to that at low elevations. These conditions shall be taken into specific account in the reliability prediction by using the environmental factor given in MIL-HDBK-217F. The analysis shall result in estimates of the mean time between failures (MTBF) and mean time to repair (MTTR), assuming that any scheduled preventive maintenance is performed.

7.2 Electromagnetic Compatibility Requirements

The ngVLA DBE/DTS work package element shall exhibit complete electromagnetic compatibility (EMC) among components (intra-system electromagnetic compatibility).

7.3 Materials, Parts, and Processes

7.3.1 Fasteners

All fasteners shall be metric except those on off-the-shelf units. The use of standard metric cross-sections for construction materials is preferred but not required.

7.3.2 Paints

Any painted coatings shall be chosen to last at least 20 years without repainting.

7.3.3 Surface Treatment

Any unpainted surfaces shall be treated against corrosion.

7.3.4 Name Plates and Product Marking

As a general rule, the main parts and all exchangeable units shall be equipped with nameplates which are visible after installation of the part/unit and which contain the following information:

- Part/unit name
- Drawing number including revision
- Serial number
- Manufacturing month and year
- Name of manufacturer

Alternatively, a system of marking based on barcodes or similar system may be used upon ngVLA approval.

For Line Replaceable Units (LRUs; see Section 11.1), it is highly desirable that the serial number of the LRU be ascertainable over the monitor and control interface (See Section 5.4)

7.3.5 Labels

All cables and switches, junction boxes, sensors, and similar equipment shall be labeled.

8 Documentation Requirements

8.1 Technical Documentation

All documentation related to the DBE/DTS work package shall meet the following requirements:

- The language used for written documentation shall be English.
- Drawings shall be generated according to ISO standards and use metric units.
- Layouts of electronic circuits and printed circuit boards shall also be provided in electronically readable form. The ngVLA preferred formats are Altium Designer files for electronic circuit diagrams and printed circuit board layouts.
- The electronic document formats are Microsoft Word and Adobe PDF.
- The preferred CAD system used is AutoDesk Inventor and/or AutoCAD.

Any deviation from the above shall be agreed to by ngVLA.

8.2 Software and Software Documentation

The DBE/DTS work package software and any other specially developed software are deliverables. The software shall be delivered in source and object form, together with all procedures and tests necessary for compilation, installation, testing, upgrades, and maintenance.

- Software must be tagged with suitable version numbers that allow identification (also on-line remotely) of a release.
- User manuals of software developed under this specification and of any other commercial software used (controllers embedded software, special tools, etc.) shall be provided.
- Software maintenance and installation upgrade documentation shall be provided.
- Full Test and Acceptance procedures shall be documented.

9 Verification and Quality Assurance

The design may be verified to meet the requirements by design (D), analysis (A) inspection (I), a factory acceptance test (FAT) or a site acceptance test (SAT). The definitions of each are given below.

Verification by Design: The performance shall be demonstrated by a proper design, which may be checked by the ngVLA project office during the design phase by review of the design documentation.

Verification by Analysis: The fulfillment of the specified performance shall be demonstrated by appropriate analysis (hand calculations, finite element analysis, thermal modeling, etc.), which will be checked by the ngVLA project office during the design phase.

Verification by Inspection: The compliance of the developed item is determined by a simple inspection or measurement.

Verification by Factory Acceptance Test: The compliance of the developed item/assembly/unit with the specified performance shall be demonstrated by tests. A FAT is performed w/o integration with interfacing systems.

Verification by Site Acceptance Test: The compliance of the developed item/assembly/unit with the specified performance shall be demonstrated by tests. SAT is performed on-site with the equipment as installed.

Multiple verification methods are allowed.

The following table summarizes the expected verification method for each requirement.

Req. #	Parameter/Requirement	D	A	I	FAT	SAT
DBE001	Clock Recovery				X	
DBE002	Coarse Sideband Separation				X	
DBE003	Digital LO for Mixer				X	
DBE004	Sub Band Selection				X	
DBE005	RFI Flagging					X
DBE006	RFI Excision					X
DBE007	Oversampling Polyphase Filter				X	
DBE008	Apply Timestamp				X	
DBE009	Data Encoding				X	
DBE010	Data Transmission					X
DBE101	Single Channel Input Data Rate	X				
DBE102	Number of Input Channels	X				
DBE103	Input Data Sample Rate/Bit Depth	X				
DBE104	Input Data Format	X				
DBE105	Output Data Format	X				
DBE106	Number of Output Channels	X				
DBE107	Output Channel Data Rate	X				
DBE108	Maximum Total Data Rate	X				
DBE109	Min DC Power Supply Voltage	X				
DBE110	Max DC Power Supply Voltage	X				
DBE111	Max Supply Current (@ –48VDC)	X				
DBE112	Operating Temperature Range	X				
DBE113	Storage Temperature Range	X				

Req. #	Parameter/Requirement	D	A	I	FAT	SAT
DBE114	Enclosure RFI Shielding @ 100 MHz				X	
DBE115	Enclosure RFI Shielding @ 1 GHz				X	
DBE116	Enclosure RFI Shielding @ 10 GHz				X	
DBE117	Physical Dimensions	X				
DBE118	Humidity	X				
DBE119	Altitude, etc.	X				
DBE120	Mean Time Between Failures	X				
DBE121	Weight	X				
DBE200	Upper/Lower Sideband Isolation		X			X
DBE201	Timestamp Jitter		X			X
DBE900	Input Power Supply voltage				X	
DBE901	Input Optical Power Monitor				X	
DBE902	Input Clock Power				X	
DBE903	Input Timing Signal				X	
DBE904	Module Temperature(s)				X	
DBE905	Electronic Serial Number				X	
DBE906	Standby Mode				X	
DBE907	Automatic Initialization				X	
DBE908	Data Transmission Link Status				X	
DBE909	Clocking System Status				X	
DBE910	Data Quality Sampling				X	

10 Appendix

10.1 Maintenance Definitions

10.1.1 Maintenance Approach

Required maintenance tasks shall be minimized. Maintenance shall be mainly performed at assembly and subassembly level by exchange of Line Replaceable Units (LRUs). LRUs are defined as units that can be easily exchanged (without extensive calibration, of sufficient low mass and dimension for ease of handling, etc.) by technician-level maintenance staff.

A step-by-step procedure for safe exchange of every LRU shall be provided in the Maintenance Manual. LRU exchange shall be possible by two trained people within four working hours. LRU replacement should be possible using standard tools identified in a maintenance manual for the Digital Backend work package.

LRUs shall be defined by the Digital Backend work package designer, depending on the design. The LRUs will be maintained by the ngVLA project (with or without industrial support).

10.1.2 Periodic Preventive Maintenance

Preventive maintenance may be performed at planned intervals in order to keep the digital backend work package operational and within its specified performance. Any required preventive maintenance should be documented in the Maintenance Manual.

10.2 Abbreviations and Acronyms

Acronym	Description
APC	Angle Polished Cut Fiber Connector
CDR	Critical Design Review
CoDR	Conceptual Design Review
CW	Continuous Wave (Sine wave of fixed frequency and amplitude)
DBE	Digital Back End
DTS	Data Transmission System
EIRP	Equivalent Isotropic Radiated Power
EM	Electromagnetic
EMC	Electromagnetic Compatibility
EMP	Electromagnetic Pulse
FDR	Final Design Review
FEA	Finite Element Analysis
FOV	Field of View
FPGA	Field Programmable Gate Array
FWHM	Full Width Half Max (of Primary Beam Power)
HVAC	Heating, Ventilation, & Air Conditioning
ICD	Interface Control Document
IF	Intermediate Frequency
KPP	Key Performance Parameters
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LO	Local Oscillator
LRU	Line Replaceable Unit
M&C, M/C	Monitor and Control
MTBF	Mean Time Between Failure
MTTF	Mean Time to Failure
MTTR	Mean Time to Repair
ngVLA	Next Generation VLA
PCB	Printed Circuit Board
RFI	Radio Frequency Interference
RMS	Root Mean Square
RSS	Root of Sum of Squares
RTP	Round Trip Phase
SAC	Science Advisory Council
SFP, SFP+, QSFP, etc.	Small Form-Factor Pluggable Optical Transceiver & Connector Standard
SNR	Signal to Noise Ratio
SRSS	Square Root Sum of the Square
SWG	Science Working Group
TAC	Technical Advisory Council
TBD	To Be Determined
UPS	Uninterruptible Power Supply
VLA	Jansky Very Large Array
WVR	Water Vapor Radiometer