ngVLA Integrated Receivers and Digitizers Design Description

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Version	Date	Author	Affected Section(s)	Reason
1	2020-01-10	M. Morgan	All	Initial Draft, based on reference design document.
2	2021-05-03	M. Morgan	All	Major update leading to conceptual design.
3	2021-06-01	M. Morgan	All	Revisions following design document review.
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Table of Contents

1 Introduction

1.1 Purpose

This document provides a description for the Integrated Downconverters and Digitizers subsystem conceptual design. It covers the design approach, functions, description of key components, interfaces, and risks associated with the conceptual design. This document will form part of the ngVLA Design documentation package.

1.2 Scope

The scope of this document covers the entire design of the Integrated Downconverters and Digitizers subsystem, as part of the ngVLA Design. It includes the subsystem's design, how it functions, and its interfaces with the necessary hardware and software systems. It does not include specific technical requirements or budgetary information.

2 Related Documents and Drawings

2.1 Applicable Documents

The following documents may not be directly referenced herein, but provide necessary context or supporting material.

Ref. No.	Document Title	Rev/Doc. No.
AD01	Integrated Receivers and Digitizers Technical Requirements	020.30.15.00.00-0003-REQ

2.2 Reference Documents

The following documents are referenced within this text:

Ref. No.	Document Title	Rev/Doc. No.
RD01	Experiments with digital sideband-separating downconversion	M. Morgan and J. Fisher, *Publications of the Astronomical Society of the Pacific*, vol. 122, no. 889, pp. 326–335, March 2010.
RD02	Unformatted digital fiber-optic data transmission for radio astronomy front ends	M. Morgan, J. Fisher, and J. Castro, *Publications of the Astronomical Society of the Pacific*, vol. 125, no. 928, pp. 695–704, June 2013.
RD03	A highly-sensitive cryogenic phased array feed for the Green Bank Telescope	D. Roshi, W. Shillue, J. Fisher, M. Morgan, J. Castro, W. Groves, T. Boyd, B. Simon, L. Hawkins, V. van Tonder, J. Nelson, J. Ray, T. Chamberlain, S. White, R. Black, K. Warnick, B. Jeffs, and R. Prestage, 32nd URSI General Assembly and Scientific Symposium, Montreal, August 2017.
RD04	SO-QSFP28-PAM4-Dxxx datasheet	https://www.smartoptics.com/wp-content/uploads/2017/10/SO-QSFP28-PAM4-DWDM-R4.0.pdf
RD05	Eoptolink 200G-400G solutions	http://www.eoptolink.com/200g-400g
RD06	Downconversion and digitization methodology for ngVLA	ngVLA Electronics Memo, no. 1

RD07	An integrated receiver concept for the ngVLA	ngVLA Memo no. 29, November 2017.
RD08	*Microwave Mixers*, 2nd ed.	S. Maas, Boston: Artech House, 1993.
RD09	*Principles of RF and Microwave Design*	M. Morgan, Norwood, MA: Artech House, 2019.
RD10	Statistical word boundary detection in serialized data streams	U.S. Patent # 8,688,617, April 1, 2014.
RD11	Digital Backend / Data Transmission System Reference Design Description	020.30.25.00.00-0002-DSN

3 Subsystem Overview

The Integrated Receiver and Digitizer (IRD) packages further amplify the signals provided by the cryogenic stage, downconvert them where necessary, digitize them, and deliver the resultant data streams by optical fiber to a moderately remote collection point from the focal plane (but possibly still inside the antenna base). From there, they can be time-stamped and launched onto a more conventional network for transmission back to the array correlator and central processing facility. Hooks are needed to provide for synchronization of local oscillators (LOs) and sample clocks, power leveling, command and control, health and performance monitoring, and diagnostics for troubleshooting in the event of component failure.

3.1 Top Level Description: Integrated Receivers and Digitizers

This subsystem consists of direct-sampled and sideband-separating modules for all telescope bands, which include warm amplification, filtering, power leveling, analog-to-digital conversion, and fiber-optic transmission. It also includes external splitters and combiners as needed to feed them from the cryogenic signal paths. Cryogenic systems and thermal transitions, as well as front-end cabling, waveguide runs, and fiber-optic signal paths outside the IRD modules themselves, are outside the scope of this work package, though interfaces must be considered.

3.2 Design Assumptions and Drivers

Paramount to the integrated receiver subsystem design is coverage of all operating bands on the telescope with the minimum number of discrete integrated modules. This minimizes construction, testing, operating, and maintenance costs as well as reducing the complexity of storage and retrieval of calibration data, and of the science data transport and timing distribution subsystems. A key limiting factor here is digitizer bandwidth and sample rate. The ngVLA has a requirement to digitize instantaneously 20 GHz of bandwidth, with a goal of sampling the entire frequency range of any given RF band simultaneously (Band 6 in particular covering more than 20 GHz of bandwidth). This is more than can be sampled instantaneously at the bit depth required with a single analog-to-digital converter (ADC) having reasonable performance and power dissipation [RD06]. Thus, the system will consist of low-loss splitters following the cryogenic front-end feeding a number of integrated receiver modules in parallel.

4 IRD Requirements

4.1 Key Requirements

A subset of the requirements that most directly drive the design is shown in Table 1. Most of these are taken from the *Key Performance Parameters* listed in the IRD Technical Requirements [AD01]. (In the case of a discrepancy, the requirements listed in the reference [AD01] are superseding.)

Parameter	Summary of Requirement	Reference
RF Input Frequency Bands	1.2–3.5 GHz 3.5–12.3 GHz 12.3–20.5 GHz 20.5–34 GHz 30.5–50.5 GHz 70–116 GHz	IRD0101 IRD0102 IRD0103 IRD0104 IRD0105 IRD0106
IF Bandwidth (after anti-alias filtering and digitization)	3.3 GHz (RF ≤ 3.5 GHz) 2.9 GHz per sideband, 2SB (3.5 ≤ RF ≤ 116 GHz)	IRD0301 IRD0302–0306
Image Rejection	≥30 dB (calibrated)	IRD0612–0616
Gain (nominal)	27–40 dB	IRD0411–0416
Gain Flatness	≤6.7 dB peak-to-peak overall, ≤2.5dB in any 100 MHz	IRD0421–0422
Gain Adjustment Range	–12/+12 dB min. (from nominal)	IRD0431
Gain Amplitude Stability	≤(0.017 dB)/(0.4 K)	IRD0441
Bands 1–6 Phase Stability	≤15 deg. absolute, with ≤2.4 deg. linear residual	IRD0451–0456
Bands 1–6 Headroom	21–26 dB P_{1dB} headroom, 41–56 dB IIP3 headroom	IRD0461–0466
Noise Temperature	≤1000 K (RF ≤ 50.5 GHz) ≤1500 K (70 ≤ RF ≤ 116 GHz)	IRD0501–0505 IRD0506
Bit Resolution	8 bits	IRD0721–0726
Physical Dimensions	40 x 80 x 160 mm	IRD1001
Mass	1.5 kg	IRD1002

Table 1. Critical requirements for Integrated Receivers and Digitizers.

4.2 RF Frequency Ranges

The total RF frequency range flows down from the system requirements, and the selection of band edges stem from a combination of engineering feasibility, hardware efficiency, and the system requirement that the band edges do not coincide with important spectral features.

The RF signal path will include a set of passive splitters and combiners to feed the correct bandwidth to each module. Note that the wider RF bands will require more than one module for complete frequency coverage. Although the conceptual design anticipates that all modules within a given RF band will be identical, this is not a requirement.

All or a subset of antennas (their number as yet undetermined) may require additional Band 4 modules to service the water vapor radiometer (WVR).

4.3 IF Bandwidth

Note that these bandwidths correspond to the bandwidth after anti-alias filtering and digitization. The LO frequencies ensure that sidebands from adjacent LOs overlap with crossover points corresponding to these IFs. Bands 2 and above are sideband-separating, using compact and inexpensive anti-alias filters with relaxed cutoff requirements. Band 1, in contrast, is direct-sampled in the first Nyquist zone, and will use a more expensive, bulky, and high-performance anti-aliasing filter. Further, all modules are dual polarization. Finally, as noted earlier, some bands will be populated with more than one module. Consequently, the numbers above represent the IF bandwidth *per sideband or Nyquist zone*, *per polarization*, and *per module*, as applicable for each band.

4.4 Image Rejection

Image rejection shall be measured with calibrated corrections applied and all internal attenuators and LOs at nominal settings. Image rejection is not expected to degrade substantially with small offsets in LO frequency or attenuator settings, so verification at these nominal settings is expected to be adequate. However, image rejection can be tested over a reasonable range of the parameter space should that be required, especially over the full gain adjustment range.

It is also notable that the implementation of sideband separation in the digital backend (DBE) may differ from that used to calibrate the IRD modules. The latter will almost certainly be performed in the frequency domain, while the former may use a time-domain finite-impulse-response (FIR) filter to implement the correction. This necessitates a mathematical translation of coefficients from those that are measured directly to those that are needed by the FIR filter.

4.5 Gain

The net warm electronic gain is required to amplify the weak output spectra of the cryogenic system to a level at the digitizers that balances quantization efficiency and dynamic range. It is specified in terms of nominal (average) value, flatness, and adjustment range. The final values of these specs will depend on the gain specification of the cryogenic amplifiers and the full-scale range of the samplers.

The nominal setting of the internal step attenuators are determined post-fabrication as that setting which most closely achieves the desired gain. The modules will further be required to have enough attenuator control range leftover to meet the gain adjustability requirements.

Gain slope is measured as the best fit line over that 80% of each IF band which minimizes its value. Gain ripple is defined as the residual variation over the same 80% bandwidth after the slope is removed from the data.

Analog gain shall be adjustable in discrete steps via integrated step attenuators or voltage-variable attenuators with discrete voltage control. The nominal setting of these attenuators shall be determined on a per module basis to most closely meet the nominal gain targets, with enough range left over to meet the requirements above. An additional 30 dB attenuator shall be available in the lower frequency bands (likely Bands 1–5) to support solar observations. At present, it is assumed the extra attenuation is not needed for the highest frequency band (Band 6).

4.6 Noise Temperature

These noise temperatures ensure that the warm electronics contribute less than 1K to the system noise temperature, assuming the cryogenic input stage has 30 dB gain (an exception is made for Band 6 for which amplifiers meeting the required noise, gain, bandwidth and dynamic range simultaneously are not available). Noise temperature shall be measured by Y-factor over the integrated noise of the IF bandwidth with the internal step attenuators at nominal setting.

4.7 Bit Resolution

Note that these represent the bit resolutions at the front-end. The correlator may requantize these data streams at lower or higher resolution levels (with appropriate care for sensitivity and dynamic range).

5 Analysis of Trade Space

The justification of the selected downconversion and digitization methodologies for the ngVLA was discussed extensively in [RD06]. The key factors driving the IRD design and the alternative approaches that were considered in that study are reiterated here for convenience.

The key performance parameters for the IRD subsystem identified in Section 4.1 (taken from the IRD Technical Requirements [AD01]) have guided the IRD module design.

5.1 Integrated Receiver Design

The IRD team at the Central Development Lab (CDL) has extensively explored reoptimized architectures for radio astronomy receivers that leverage modern advances in integrated electronics and digital signal processing. These two general technologies are deemed to be mutually complementary, in that numerical digital processing (with appropriate calibration) provides accuracy and flexibility that is far superior to pure-analog designs (e.g. the calibrated requirements IRD0612–0616), while integrated construction of the residual analog hardware delivers uniformity and stability of performance (IRD0441, IRD0451-0456) to ensure the greatest precision and longevity of digital calibrations.

The two guiding principles of the integrated receiver development program since the beginning have been

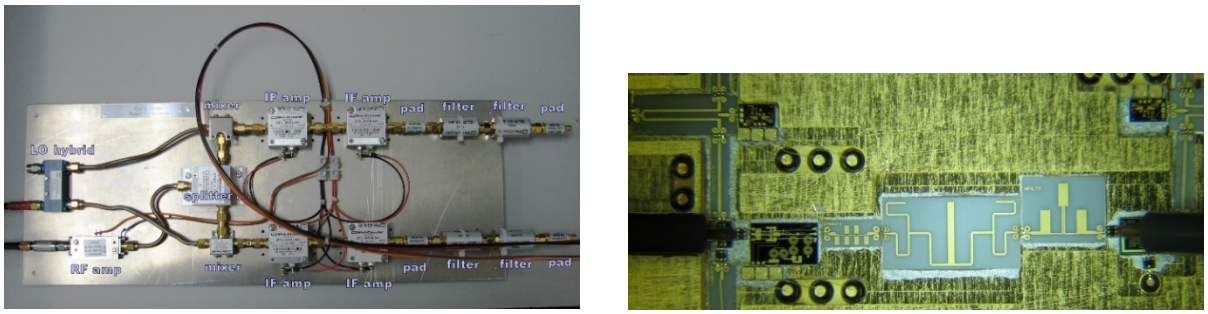
- to digitize signals from the sky as close as possible to the focal plane of the telescope, deferring as much functionality as is feasible into the digital domain, and
- to maximize integration, especially across the traditional boundaries of analog, digital, and photonic components, so that the greatest performance could be achieved in a compact, power-efficient, field-replaceable unit.

Early digitization, compactness (IRD1001 and IRD1002), and power efficiency, more than simply conveniences, have significant performance and life-cycle cost advantages, as will be described in the following sections. These considerations are what have driven the design to the architecture which was ultimately selected for the ngVLA [RD07].

5.1.1 Strengths and Weaknesses

Integrated electronics, like any technology, has both strengths and weaknesses that differ from those of earlier approaches which drove the architecture of previous generations of instruments. It is a very common mistake to repurpose a preexisting block diagram, optimized around the strengths and weaknesses of older technology, to be implemented with integrated components without taking into account those differences.

In this case, the older generation of technology comprised individually packaged and connectorized components (amplifiers, mixers, etc.) plumbed together with coaxial cable or waveguide in isolated analog, digital, and photonic subassemblies. As an example, a photograph of a traditional, connectorized analog sub-assembly is shown in Figure 1(a).



(a) (b)

Figure 1. Examples of (a) a traditional sub-assembly of individually packaged, connectorized components, and (b) an integrated module containing semiconductor chips.

Integrated modules, in contrast, at high frequency would comprise multiple semiconductor die—Monolithic Microwave Integrated Circuits (MMICs)—as shown in Figure 1(b), or at lower frequency, high density circuit boards of surface-mount components. In practice, most integrated modules will incorporate a mix of bare die (for the LO and RF) and integral circuit boards (for baseband, digital, and photonic parts) as required by the application.

The relative strengths and weaknesses of these two approaches is summarized in the Table 2.

Technology	Strengths	Weaknesses
Connectorized	• ease of assembly and test • hand-tuned performance • high part-to-part isolation • low development cost	• bulky • prone to pass-band ripple and slope • poor repeatability • high replication cost
Integrated	• compact • amplitude & phase stability • uniformity/repeatability • low replication cost	• needs special equipment • higher loss, lower *Q* • prone to leakage & cross-talk • high development cost

Table 2. Comparative strengths of connectorized versus integrated technology.

The low replication cost and repeatability of performance offered by integrated techniques is reason enough to select them for a large-*N* array such as the ngVLA (consider the lifecycle optimization requirement, IRD1202), but the weaknesses, particularly the propensity for cross-talk between elements, must be a driving factor in the architectural design of the integrated modules—in fact, it was pivotal in the decision to use single-stage, direct-to-baseband downconversion for this project.

5.1.2 Advantages of Compactness

One of the aspects of the IRD program which is frequently underappreciated is the importance that is placed on compactness. While it is clear that the present trend in radio astronomy that dish diameters are shrinking, even as the number dishes in an array is growing, and therefore the room available near the focal plane of such a dish to support the electronics for an ever-increasing operational bandwidth is limited (IRD1001–1002), once the electronic package is small enough to fit, many assume that there is no advantage to making it any smaller.

In fact, there are significant performance as well operational advantages to having a more compact module. It is critical for high-performance, wideband systems to maintain flat gain (IRD0421–0422) and phase structure so that sensitivity and dynamic range (IRD0461–0466) can be optimized simultaneously. Tighter integration ensures that the electrical length between components internally is minimized so as to avoid the creation of rapid pass-band ripples due to standing waves. Smaller modules, in turn, can be placed closer to the cold electronics package, reducing the external cabling and loss slopes, while easing the stabilization of temperature.

Operationally, the compactness if the IRD modules is an enabling factor that makes it feasible to treat the large front-end antenna electronics package as a unified Line-Replaceable Unit (LRU).

5.1.3 Power Dissipation Drives Life-Cycle Cost

Another important but underrated aspect of the IRD program is the pursuit of the lowest possible power dissipation. While this reduces the overall power consumption of the antenna (probably negligible compared to other subsystems, say, the cryogenics), it more importantly improves the lifetime of the active components (IRD1101). Considering that the integrated modules incorporate all of the functions of the warm analog electronics, the samplers, and the fiber-optic transceivers into one small package, there is quite a bit of hardware packed into them, so it is essential for thermal management that each component dissipates as little power as possible.

5.1.4 Challenges Associated with Integration

As acknowledged in Table 2, there are certain weakness associated with integrated module construction which must be addressed. Paramount among these is the possibility of leakage and cross-talk between components. This is a driver of the downconversion scheme selected, which will be discussed in Section 5.2. It also incurs the risk of self-generated RFI, which drives the selection of a low-overhead digitization scheme which is described in Section 5.3.3.

The IRD program has worked extensively on these issues, and a number of module design techniques and standards have been found to be effective in mitigating these risks. In addition to the selection of downconversion and digitization schemes, the housing is designed to channelize parallel analog signal paths (RF and IF), while the analog and digital electronics are isolated in separate cavities. These measures also help to minimize the radiated emissions of the IRD modules.

5.2 Downconversion

A significant portion of the ngVLA's 1.2–116 GHz frequency range is beyond the reach of practical digitizers, so the spectrum must first be downconverted to a lower frequency. A critical performance parameter of analog downconverters is the suppression of leakage from undesired image bands (IRD0612–IRD0616). A number of approaches have been developed over the years to achieve this. These will be summarized and discussed in the following subsections.

5.2.1 Single-Stage Image-Filtered

Perhaps the simplest approach is simply to attenuate the undesired image frequencies prior to downconversion, as illustrated in Figure 2(a) (next page).

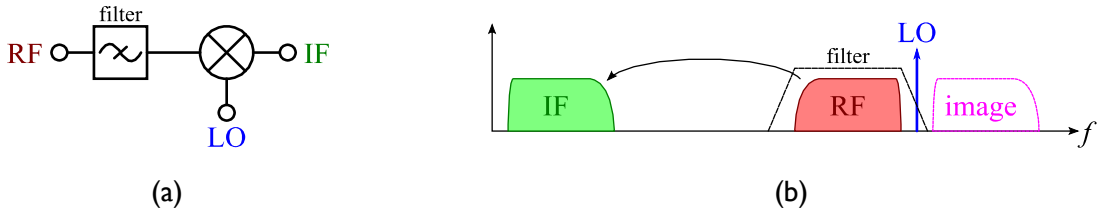


Figure 2. (a) Single-stage mixer with image-rejection filter. (b) Spectral diagram.

The frequency bands associated with this technique are shown in Figure 2(b), where a lower-sideband downconversion is shown for illustration. When downconverting from a fairly high-frequency, like ngVLA Band 6 (70–116 GHz), this approach demands a very high-selectivity filter to cutoff sharply between the upper end of the RF band and the lower end of the image band. Typically, this would have to be a cavity or dielectric resonator filter, which are large and expensive. To alleviate the selectivity requirement, the IF bandwidth could be pushed higher in frequency, spreading the RF and image bands further apart, but this then demands a very high-speed digitizer, or at least one that has an exceptionally fast track-and-hold stage, driving up the power dissipation.

Further, unless the sampler can digitize the entire RF bandwidth provided by the feed in one shot (rarely the case in radio astronomy), the filter will have to be tunable to cover the image bands which shift laterally as the LO is swept, and will undoubtedly overlap part of the RF input range. Pushing the IF frequency high enough so that there is no overlap between image and feed frequencies is not even remotely feasible.

5.2.2 Multistage

One way to alleviate the filtering selectivity and tuning requirements is to employ two-stage downconversion, such as that shown in Figure 3.

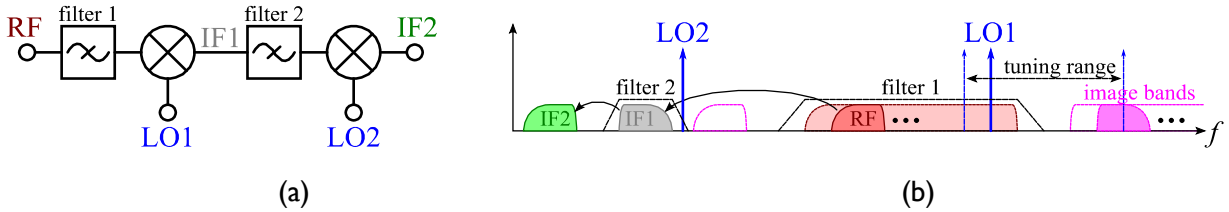


Figure 3. (a) Two-stage downconversion. (b) Spectral diagram.

The wide RF feed frequency range is first filtered with a relatively low-selectivity, fixed filter (filter 1 in the figure). A first local oscillator, LO1, is swept through the upper part of the band and above, such that a sliding window of RF bandwidth is downconverted to relatively high intermediate frequency, IF1. The lowest possible image for this downconversion (shown in magenta at the far right of the figure) is still outside of the RF bandwidth as well as the filter1 passband. The high IF1 is then downconverted with a second, fixed local oscillator, LO2, after another fixed filter, filter 2. Although the final intermediate frequency, IF2, is low enough to be digitized effectively, it was downconverted from a more moderate frequency, IF1, than the original RF band, so that filter 2 may still have relatively low selectivity. In this way, both filters are fixed and need not have exceptionally high selectivity.

There are costs, however, beyond just the increase in complexity (which is itself a factor). For one, the first LO frequency must extend well above the highest operational frequency of the telescope. More importantly, however, the presence of two local oscillators feeding into the same integrated analog signal path increases the population of spurious mixing products (IRD0631). Recall that one of the disadvantages of integrated construction is the relatively poor isolation between components and the propensity for leakage or cross-talk. This makes it difficult to sufficiently suppress higher-order mixing products, and the

fact that LO1 must be tunable makes them impossible to avoid in frequency space—they are literally everywhere. While this approach has been used in non-integrated receivers, it is clearly not a good choice for integrated architectures.

5.2.3 Analog Sideband-Separating

An attractive alternative is the sideband-separating mixer [RD08], shown in Figure 4.

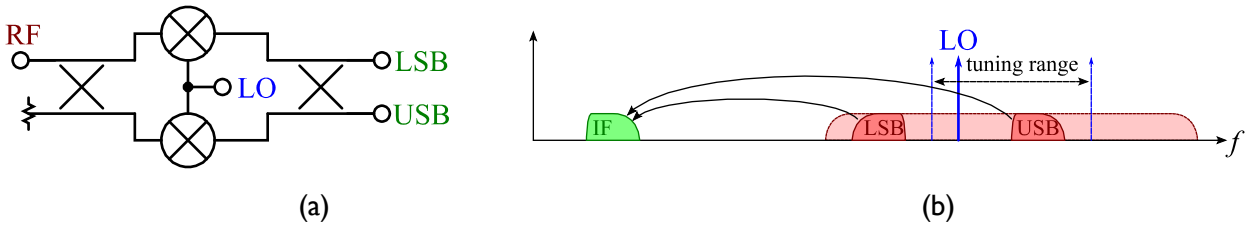


Figure 4. (a) Sideband-separating mixer. (b) Spectral diagram.

Rather than prefiltering the image bands, both are downconverted simultaneously through a clever arrangement of mixers, splitters, and quadrature hybrids which use phasing to deliver the two sidebands separately to independent ports.

The first quadrature hybrid may appear on either the RF or LO port [RD09], but a hybrid is always required on the IF output. Analog hybrids of this type cannot be made to work at DC, so there is a limit to how low in frequency the IF range may go. Although hybrids with decade bandwidths have been demonstrated, they are lossy and have significant gain slope (IRD0421), as well as being physically enormous (IRD1001) if made for the first Nyquist zone of any practical digitizer. Generally, analog sideband-separating mixers are therefore designed for at least the second Nyquist zone, so that the hybrid is required to cover at most one octave (unless the mixer is followed by other mixing stages prior to digitization, as is the case in ALMA). This of course requires the digitizer to have a wideband track-and-hold stage supporting the second-Nyquist frequency range, at moderate cost to power dissipation, and placing additional constraints on the digitizable bandwidth.

Furthermore, even over an octave bandwidth, it is difficult for the IF quadrature hybrid to maintain accurate amplitude and phase balance. Image rejection ratios of even 15 dB can be a challenge for such systems if wideband operation is desired.

5.2.4 Digital Sideband-Separating

To mitigate these issues, the IF hybrid may be implemented numerically, after digitization, as shown in Figure 5.

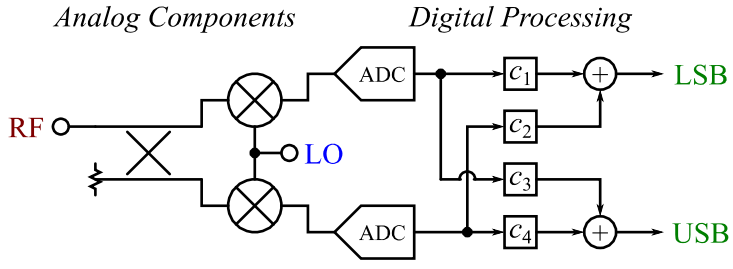


Figure 5. Sideband-separating mixer with a numerically implemented IF quadrature hybrid using calibrated complex-gain coefficients.

Not only can this "digital hybrid" operate down to arbitrarily low frequency, thus allowing the sampler to work directly at baseband, it is largely immune to the amplitude and phase errors of pure-analog implementations. The complex coefficients (c_1 to c_4 in the figure) can be calibrated to correct for the imbalances of the preceding analog components, thus achieving nearly perfect sideband separation [RD01]. Performance in this area is limited by the sensitivity of the calibration procedure, which shall be carried out in the lab, and the longevity of those calibrations which is greatly enhanced by the integrated construction of the analog components. For the ngVLA's requirement of 30 dB image suppression (IRD0612–0616), it is likely that the laboratory calibration will be effectively permanent, needing updates only when a part is repaired or replaced.

5.3 Digitization and Data Transfer

Once downconverted, the analog signal must be digitized for transmission away from the focal plane, and ultimately back to the central signal processor. Although some telescopes transmit analog signals from the focal plane to other parts of the telescope (say, the base or pedestal) prior to digitization, this is not considered a desirable solution for numerous reasons. Coaxial cables over the lengths required would introduce a great deal of loss and gain slope (IRD0421). Analog fiber-optic links, on the other hand, even short ones, are extremely noisy and prone to dynamic range issues (IRD0461–0466), especially for wide analog bandwidth. Either option further exposes the signal path to temperature fluctuations and flexure at the telescope axes which introduce phase variations (IRD0451–0456, IRD0471–0476) that ultimately must be tracked and taken out. By digitizing early, we protect the information from any kind of corruption during transport.

5.3.1 Direct-Sampled

Some designers favor direct-sampling at relatively high-frequencies (in high-number Nyquist zones), as shown in Figure 6,

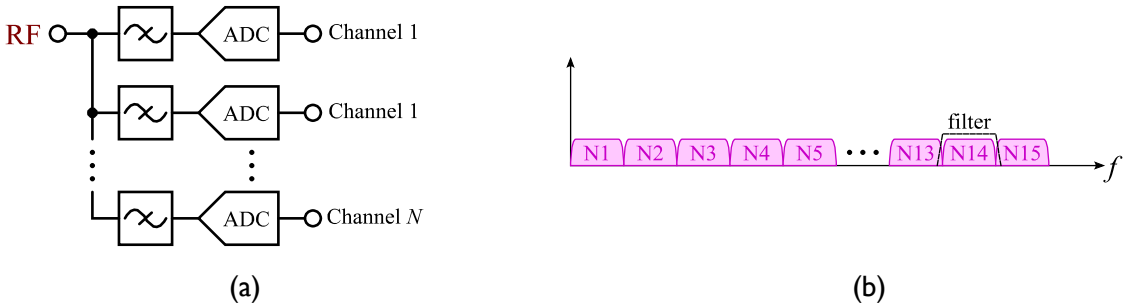


Figure 6. (a) Direct-sampling architecture. (b) Filtering a high-level Nyquist zone.

thus bypassing the downconversion altogether. While appealing for its architectural simplicity, it requires an ADC with an extraordinarily high-frequency input stage—inevitably power-hungry with compromised performance—as well as a suite of very high-performance filters which are bulky (IRD1001,1002) and expensive (IRD1202), and yet still sacrifice some bandwidth at the zone edges. These drawbacks aside, it is highly unlikely that sampling could be achieved as high as ngVLA's Band 6, requiring one of the aforementioned downconversion schemes for at least that band anyway.

5.3.2 Conventional ADC Boards and Data Formatters

For the bandwidths that we require, conventional ADC's must be interfaced directly to power hungry FPGA's to do the formatting (bit-scrambling, packetizing, etc.) required of industry standard data links.

Even the modern JESD204B standard for so-called "serial-output" ADCs[1] is meant only for short-distance communication, typically from ADC to FPGA on the same circuit board or from a mezzanine card to its motherboard. Long-distance communication between the ADC and FPGA, even tens of meters, is out of the question, due to the need to keep synchronized multiple serial lanes and frame clocks.

In addition to the bulk (IRD1001,1002) and power dissipation associated with implementing these schemes, especially for broad-bandwidth data, the localized buildup of high-speed digital electronic components increases the risk of self-interference (IRD0631), both through emission and conduction via supply buses and grounds. While we are assuming the risk of integrating analog and digital electronics in the front-end, it is nevertheless advantageous to keep the digital electronics to a minimum.

5.3.3 Unformatted Links and the Serial ADC

To that end, the IRD group has conducted extensive research in the use of unformatted serial links for transmission of digitized radio astronomy data, without the overhead associated with commercial protocols [RD02]. While conventional data transmission systems are optimized to work with any kind of data—whether it be compressed streaming video or mostly-empty files having long strings of zeros—we know a great deal a priori about the content of our signals. To a high degree of accuracy, they will essentially comprise Gaussian-distributed white noise (dominated in most cases by the noise of the cryogenic amplifier, if not the source on the sky).

We can use these properties to our advantage by exploiting the natural statistics of our signal as its own "formatting" without the need of high-speed digital electronics in the front-end, aside from the digitizer itself and a bare-bones serializer to drive the laser [RD10]. There are efficiencies to be gained from this in the front-end, especially if the sampling and serialization functions can be integrated onto the same piece of silicon, as illustrated in Figure 7.

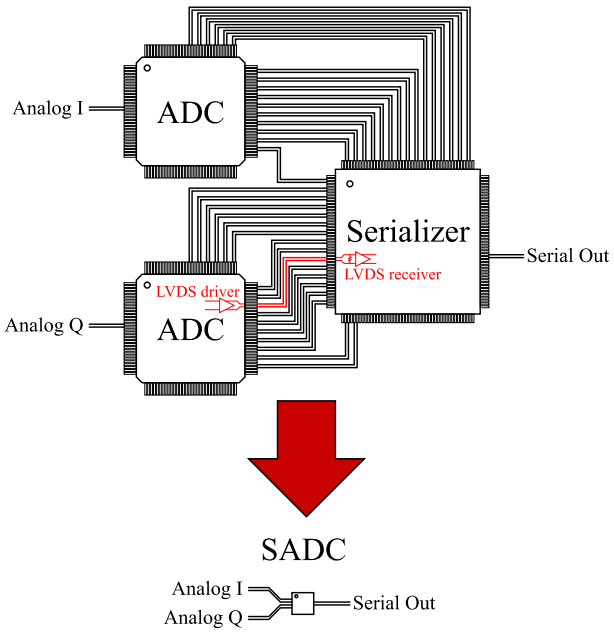


Figure 7. Integration of the sampling and serialization functions in a Serial ADC (SADC) for an order of magnitude improvement in footprint, while saving power in the interface between them.

[1] These standards typically multiplex the sample stream to several independently serial outputs, along with parallel clock channels, making it more accurately a combination of serial and parallel communication.

The surface-mount packages for common ADCs are typically on the order of an inch square, not because of the size of the chip inside, but because of the number of pins that must be accommodated around the periphery to support a parallel (and often multiplexed) interface. Even the aforementioned JESD204B devices and those packaged in ball-grid arrays (BGAs) are still among the largest devices a high-speed circuit board will contain, aside perhaps from the monstrous FPGA itself. In our application, the traces from this wide interface are immediately collected again in a serializer which reduces them all once more to a single differential output, connected to a laser driver. By integrating these two parts on a single chip, we eliminate the vast majority of intermediate pins, giving us an order of magnitude reduction in footprint on the circuit board (IRD1001).

Furthermore, the interface between chips using conventional parts comprises resistively-terminated transmission lines—most commonly a protocol known as low-voltage differential signaling (LVDS). Clearly wasteful of power, they are nevertheless required due to the (a priori) unknowable parasitics of the traces on the board. On-chip, the connections between ADC and serializer can be wired directly, gate-to-gate, without any loss of power except when switching.

In early IRD prototypes incorporating all the warm-electronics of a radio astronomy front-end—post-amplification, power leveling, downconversion, filtering, digitization, and fiber-optic transmission—about 75% of the power was dissipated in the digital electronics, and that was only at a fraction of the sample rate and serial rate needed for ngVLA. Recent work has revealed that industry-compatible interfaces for 56 Gbps serial data transceivers will preclude the elimination of formatting entirely (64b/66b encoding will still be included), but nevertheless the Serial ADC concept is expected to dramatically improve the trade-off of speed versus footprint and power.

5.4 Conclusions of Trade Study

The preceding analysis has shown that an integrated approach offers tremendous advantage in terms of size, weight, and power (SWaP) as well as replication cost and stability, all of which are critical to the ngVLA. Stability and spectral purity in the context of an integrated receiver further drive the design toward a minimal downconversion strategy with early digitization and fiber-optic transmission having low digital overhead.

For these reasons, and in light of the key performance specifications identified in Section 4.1, we have selected for the ngVLA's conceptual design a single-stage direct-to-baseband I/Q downconversion with calibrated numerical sideband-separation, followed by a low-overhead serial-ADC driving an unformatted fiber-optic link. This combination is believed to provide the best performance for cost and manufacturability, in accordance with the system engineering requirements and the general guidelines laid out in Section 4.

6 IRD Conceptual Design

The design of the ngVLA IRD modules evolved from an internal research program (the Integrated Receiver Development program), which has been perfecting the techniques used in their construction for more than a decade at the time of this writing. The original program aimed to leverage the advantages of modern electronic integration and digital signal processing, to digitize as closely to the antenna feed-point as possible without comprising ultimate performance, and to re-optimize legacy receiver architectures in light of these new techniques and in anticipation of future telescope facilities such as the ngVLA.

Integration and digital signal processing (DSP) are deemed complementary in this program, in that the latter provides for greater signal fidelity and precision in concert with detailed calibrations than purely analog techniques, while the former guarantees the long-term stability and uniformity of those calibrations.

This resulted also in compact, low-power, field-replaceable receiver units which were a perfect fit for ngVLA's maintenance and operability requirements.

As described in Section 5.2, due to the compact, integrated construction, it is unwise to perform downconversion in multiple steps. Integrated modules, though they have many advantages, do not typically have as good of isolation between inputs as individually connectorized components. Multiple local oscillator tones, then, tend to produce a copious spread of mixing products that inevitably lead to spurious tones in the output spectrum.

We therefore process the higher frequency bands using a single-stage, direct-to-baseband downconversion with in-phase and quadrature (I and Q) channels. These channels are then processed numerically in the back-end to produce upper and lower sidebands more precisely than an analog hybrid ever could. The IRD program has a long track record of producing clean output spectra with 50–60 dB sideband suppression using this technique (e.g. [RD01]).

At the lowest frequency band, downconversion is an unnecessary complexity, usually requiring a triple-balanced mixer to achieve the required IF bandwidth while isolating it from the RF and LO inputs which overlap with it in frequency space. For this band, instead, we use a direct-digitization approach in the first Nyquist-zone of the sampler.

To minimize power requirements and the risk of self-interference with integrated digital and high-gain analog electronics, the IRD program developed a novel approach to digital data transmission. Specifically, it delivers unformatted digital data streams over optical fiber without any of the usual bit-scrambling or packetizing used in the data-communications industry (64b/66b encoding may still be used, as this appears to be deeply ingrained in the operation of 56 Gbps serial transceivers). This "low-overhead" digital design [RD02] relies on the statistical characteristics of Gaussian-distributed white noise—which dominates the signal in any properly designed radio astronomy receiver, even those heavily laced with man-made interference—to parse the bit stream at the receive-end of the fiber, away from the focal plane where power and interference are less harmful. Numerous demonstrations of this concept have been built and proven, and it has now been fielded in a technology demonstrator on the Green Bank Telescope [RD03].

A critical element of the low-overhead serial link described above is the Serial ADC (SADC). This essentially marries a conventional ADC and a conventional Serializer (or SerDes) without any of the usual, intervening, complex digital logic. Implemented to date using off-the-shelf parts, fully realizing this idea's potential benefits relies on integrating these two components on a single piece of Silicon. This avoids the wasted size, weight, and power (SWaP) associated with chip-to-chip parallel interfaces. The functional components of this proven technique (the ADC and the Serializer) already exist commercially, making this a development with low technical risk, but one that requires a significant investment in producing the ASIC.

The unformatted fiber optic links will likely not interface directly with the array correlator/signal processor. Rather, they will interface with the Digital Back-End (DBE) inside the antenna, and from there to the long-distance data transmission subsystem which will carry the data the rest of the way on more conventional (possibly commercial) links.

6.1 IRD Overview and Block Diagram

A block diagram of the Integrated Receivers/Downconverters and Digitizers Subsystem is shown in Figure 8 with all electrical interfaces included. Note that both the LO and clock frequencies shown are nominal values; small offsets from these values are allowed on a module-by-module basis (more likely in practice antenna-by-antenna) to facilitate suppression of spurious signals. The internal block diagrams of the

sideband separating (2SB) and direct-sampled (DS) receiver modules appear in Section 0. The gray boxes provide information about subsystem inputs and outputs.

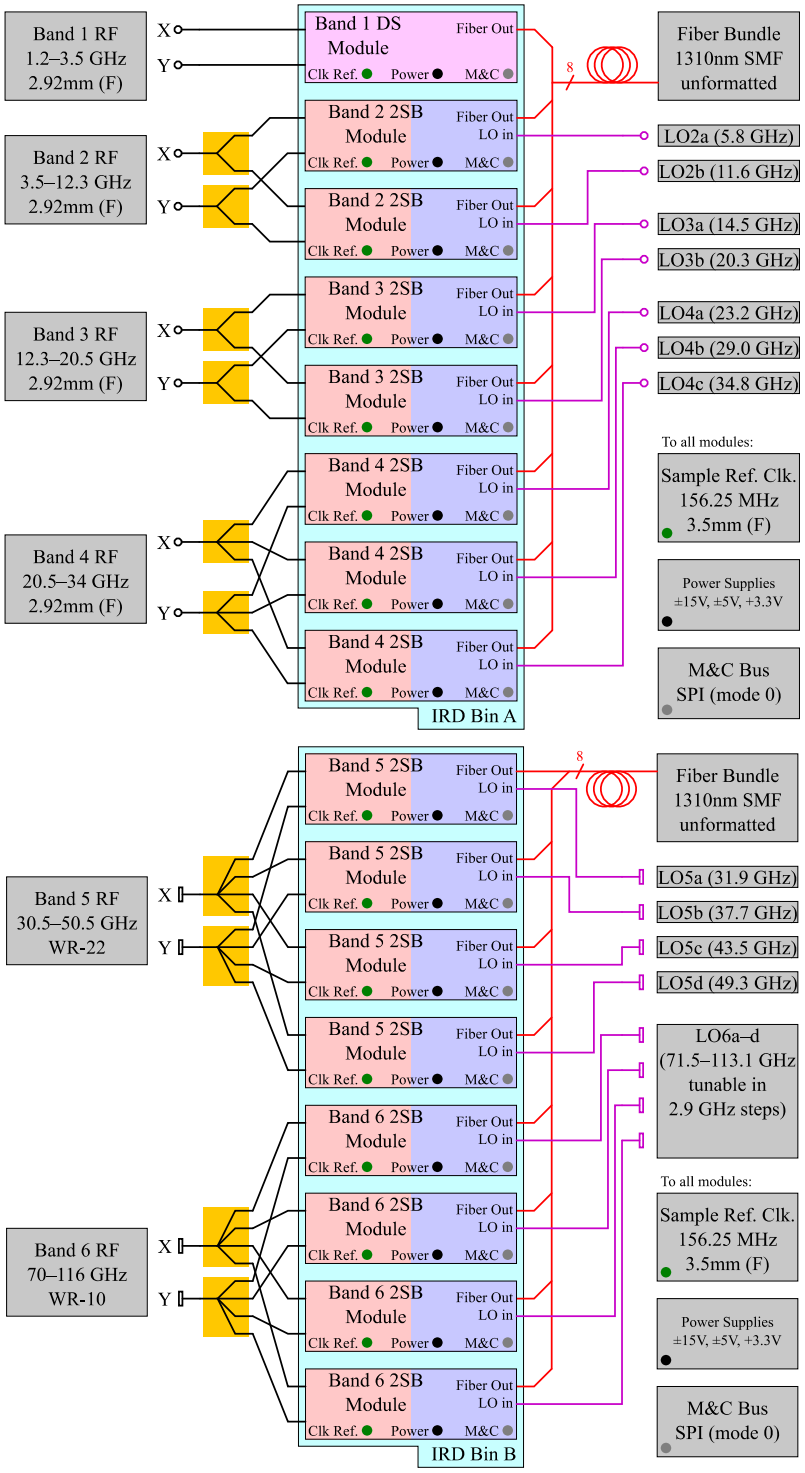


Figure 8 - Block diagram of Integrated Receivers/Downconverters and Digitizers subsystem, bin A (Bands 1–4) and bin B (Bands 5–6).

Note that the current implementation does not call for a full-speed digitizer clock to be input to the IRD module, only a 156.25 MHz reference (plus offsets on the order of 5 MHz). Although the SADC is still under development, there is reason to believe that integration of the ADC and the serializer onto one chip could be simplified if the necessary clocks and clock-phases needed for both were generated at the same time from a common PLL block, an option which would not exist for systems in which the ADC and serializer are separate. It also simplifies the packaging if the sample clock does not need to be input directly through external pins. Our initial investigations have suggested that clocks of the appropriate quality (e.g. in terms of jitter) can be included on the chip. This may also simplify isolation of the sample clocks from the analog components, reducing self-induced RFI and radiative emissions, since the high-frequency interconnections on-chip will most likely be differential, whereas external high-frequency interconnects (e.g. coaxial) are more often single-ended.

It should also be noted that the RF interfaces are coaxial up to Band 4, and waveguide for Bands 5 and 6. It may be possible to use coaxial cable for all receiver bands, with 2.4 mm coax connectors in Band 5, and 1 mm connectors in Band 6. This would improve serviceability of the Dewar and IRD modules within in the antenna electronics assembly. The coaxial cables in Band 6 are most critical, and would have to be kept as short as possible, say 10–20 cm. An estimation of the performance of a 15-cm length of cable using a high-performance (but expensive) product from W.L. Gore is given in Table 3. The tradeoff associated with this option should consider not only the excess loss, but the slope introduced across the band as well.

Frequency (GHz)	Connector Loss (ea.)	Loss per ft.	Total Insertion Loss	Return Loss
70 GHz	0.3 dB	3 dB	2.1 dB	14 dB
110 GHz	0.3 dB	4.1 dB	2.7 dB	14 dB

Table 3. Estimated performance of high-end 1-mm coaxial cable for Band 6.

Note that it is likely the splitters in the IRD subsystem would still utilize waveguide interfaces, and consequently the IRD modules themselves would use waveguide as well. Good coax-to-waveguide adapters in this frequency range typically have return loss around 16 dB.

6.2 IRD Components

By far, the most significant major components of the IRD subsystem are the receiver modules. As described above, the architecture and frequency distribution of these receiver modules have been designed to cover the required bandwith with the minimum amount of hardware. Figure 9 and Table 4 summarize the resulting frequency plan. Note that antennas outfitted with a water vapor radiometer may need an additional two Band 4 modules, not shown in Figure 9.

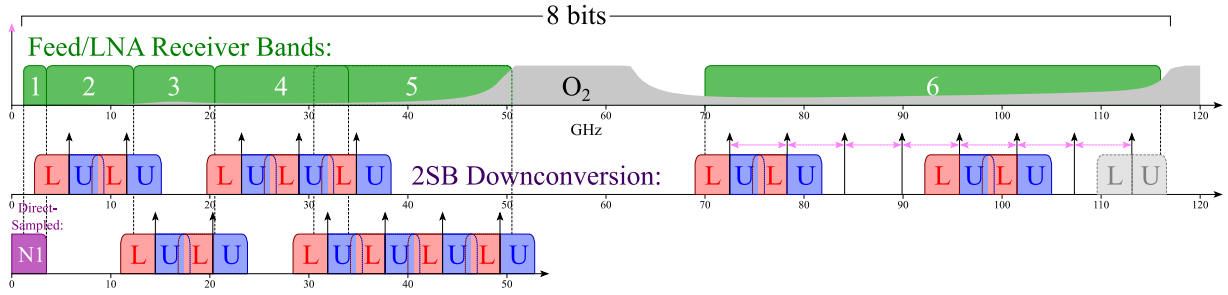


Figure 9 - Integrated Receiver/Downconverters and Digitizers frequency plan.

Band	RF Range (GHz)	Type	# bits	Sample Rate (GS/s)	LO (GHz)	LSB (GHz)	USB (GHz)
1	1.2–3.5	DS	8	7	--	0.0–3.3	
2	3.5–12.3	2SB	8	7	5.8	2.9–5.8	5.8–8.7
		2SB	8	7	11.6	8.7–11.6	11.6–14.5
3	12.3–20.5	2SB	8	7	14.5	11.6–14.5	14.5–17.4
		2SB	8	7	20.3	17.4–20.3	20.3–23.2
4	20.5–34	2SB	8	7	23.2	20.3–23.2	23.2–26.1
		2SB	8	7	29.0	26.1–29.0	29.0–31.9
		2SB	8	7	34.8	31.9–34.8	34.8–37.7
5	30.5–50.5	2SB	8	7	31.9	29.0–31.9	31.9–34.8
		2SB	8	7	37.7	34.8–37.7	37.7–40.6
		2SB	8	7	43.5	40.6–43.5	43.5–46.4
		2SB	8	7	49.3	46.4–49.3	49.3–52.2
6	70–116	2SB	8	7	72.5	69.6–72.5	72.5–75.4
					75.4	72.5–75.4	75.4–78.3
					78.3	75.4–78.3	78.3–81.2
					81.2	78.3–81.2	81.2–84.1
		2SB	8	7	84.1	81.2–84.1	84.1–87.0
					87.0	84.1–87.0	87.0–89.9
					89.9	87.0–89.9	89.9–92.8
					92.8	89.9–92.8	92.8–95.7
		2SB	8	7	95.7	92.8–95.7	95.7–98.6
					98.6	95.7–98.6	98.6–101.5
					101.5	98.6–101.5	101.5–104.4
					104.4	101.5–104.4	104.4–107.3
		2SB	8	7	107.3	104.4–107.3	107.3–110.2
					110.2	107.3–110.2	110.2–113.1
					113.1	110.2–113.1	113.1–116.0
					116.0	113.1–116.0	--

Table 4. IRD frequency plan in tabular form. Note that Band 6 has four 2SB modules selecting between sixteen LO's.

6.2.1 Sideband-Separating (2SB) Receiver Modules

A conceptual block diagram of a typical 2SB receiver module is shown in Figure 10. Each module has two RF inputs, one for each polarization. These inputs are broadband filtered to limit the power to downstream components, then amplified.

Preferably following the warm RF amplifier is a step attenuator for level control. This ensures that any changes here have minimal effect on the calibration coefficients for sideband-separation. At the highest frequencies, where step-attenuators may not be readily available, this level-control could be moved into the IF signal path. In that case, the M&C software should be programmed to step the attenuators in the I and Q signal paths synchronously after initial balancing in the lab—again, to ensure minimal impact on the calibration coefficients. Although some uncorrected amplitude imbalance will result from non-uniformity of the step-sizes of the two attenuators, the effect should be sufficiently small that the modules will still easily meet the sideband-rejection specification. All 2SB modules will support a power adjustment range of ±12 dB from nominal. The lower frequency bands may need an additional 30 dB switchable attenuator to support solar observing. This 30 dB of extra attenuation will undoubtedly degrade the noise figure, but this is not a concern for the solar-observing scenario.

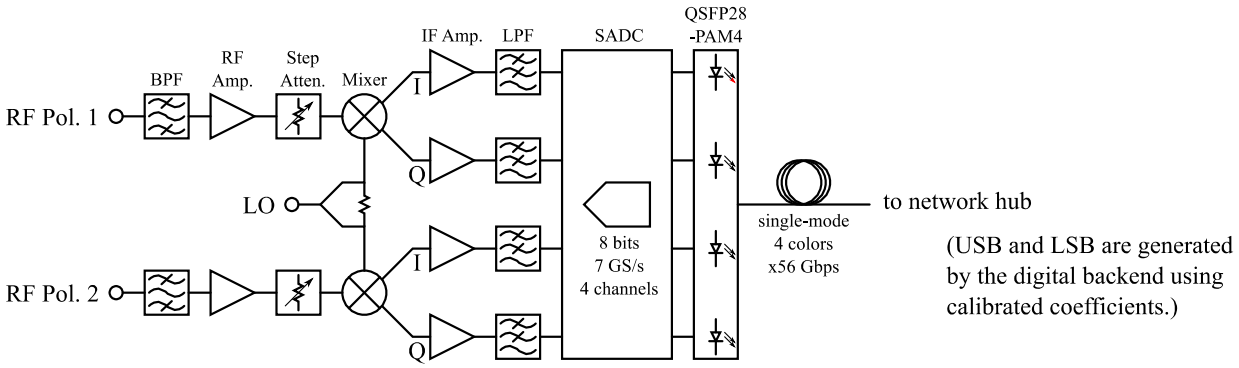


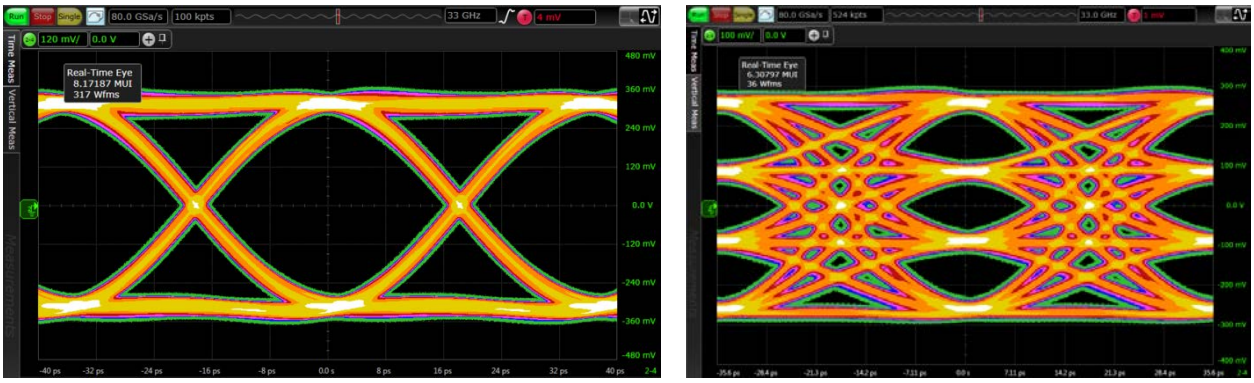
Figure 10 - Block diagram of a sideband-separating (2SB) receiver module. Note that the actual data streams delivered from the module represent I and Q channels; the USB and LSB will be generated in the digital backend using calibrated coefficients provided by the IRD team.

The mixers implement a single-LO, direct-to-baseband, I/Q downconversion. Additional warm-amplification and anti-alias filtering is present at baseband. This is followed by the Serial-ADC (SADC) chip described earlier. They will either be two dual-channel SADCs or a single quad-channel SADC to capture I and Q from both polarizations. The SADC chip will use 8-bit sampling at 7 GS/s.

This sample rate and bit depth are compatibile with the emerging industry standard serial rate of 56 Gbps per lane. These serial outputs are therefore fed into a quad-channel fiber-optic transceiver capable of transmitting 56 Gbps per lane, where four optical wavelengths are combined onto a single fiber. Although relatively new, such transceivers conforming to the QSFP28 form-factor (shown in Figure 11) are now becoming available with reaches of 500m up to 80 km [RD04, RD05]. These transceivers modulate the optical carrier at 28 giga-symbols per second using four-level pulse-amplitude modulation (PAM4), thus achieveing the serial rate 56 Gbps.

A comparison of the eye-diagrams for the more common binary NRZ modulation and the PAM4 modulation are shown in Figure 12. The implementations of our serial link in actual telescope hardware to date have been limited to the NRZ waveform, but the PAM4 waveform should be equally robust.

Figure 11 - Quad Small Form-Factor Pluggable (QSFP28) optical transceiver.

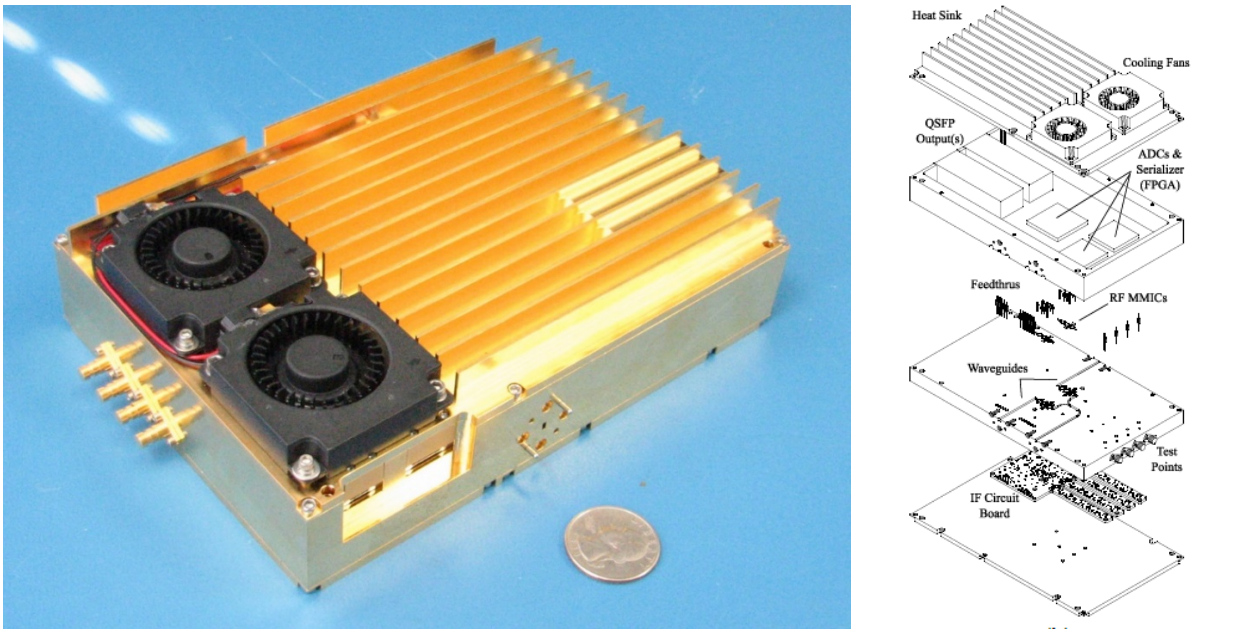


(a) (b)

Figure 12 - Comparison of (a) binary NRZ and (b) PAM4 optical modulation schemes.

Although the SADC chip, critical to realizing the SWaP benefits of the proposed design, is not yet available, prototyping on fully functional (but not full-spec) receiver modules has already begun. Figure 13 shows an example. The internal details of the construction are shown in the exploded view in Figure 13(b).

This dual-polarization module operates in W-band (75–110 GHz) and may be considered an early prototype for the ngVLA Band 6. It utilizes a Kintex7 FPGA to implement the unformatted serialization of the ADC outputs at 8 Gbps. When the SADC chip becomes available, the same function as this FPGA plus the two ADCs will be implemented on a single chip in a very small package and consuming less power. This module has two QSFP output connectors (which are really redundant since only one has enough channels to service the whole module).



(a) (b)

Figure 13 - Prototype W-band IRD 2SB receiver module. (a) Photo. (b) Exploded view of internal construction. Note that this is only a prototype. The cooling fans are needed here since the power-saving Serial ADC ASIC was not yet available. The conceptual design version will be smaller, consume less power, and be cooled without fans by attachment to a temperature-controlled plate.

Preliminary drawings of a coaxial Band 3 module are shown in Figure 14 through Figure 16, illustrating the construction of the housing, layout of the internal high-frquency chips, and IF circuit board for baseband processing. The digital/photonic circuit board has yet to be designed, awaiting completion of the SADC.

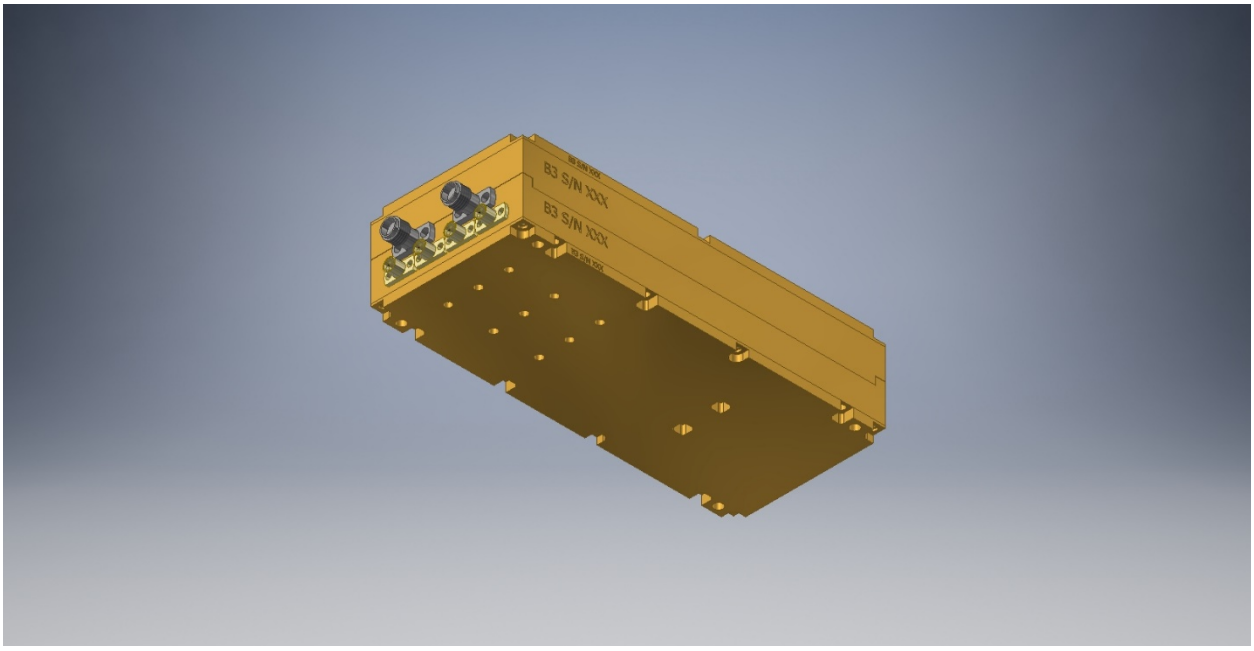


Figure 14. Preliminary design drawing of a coaxial Band 3 IRD module.

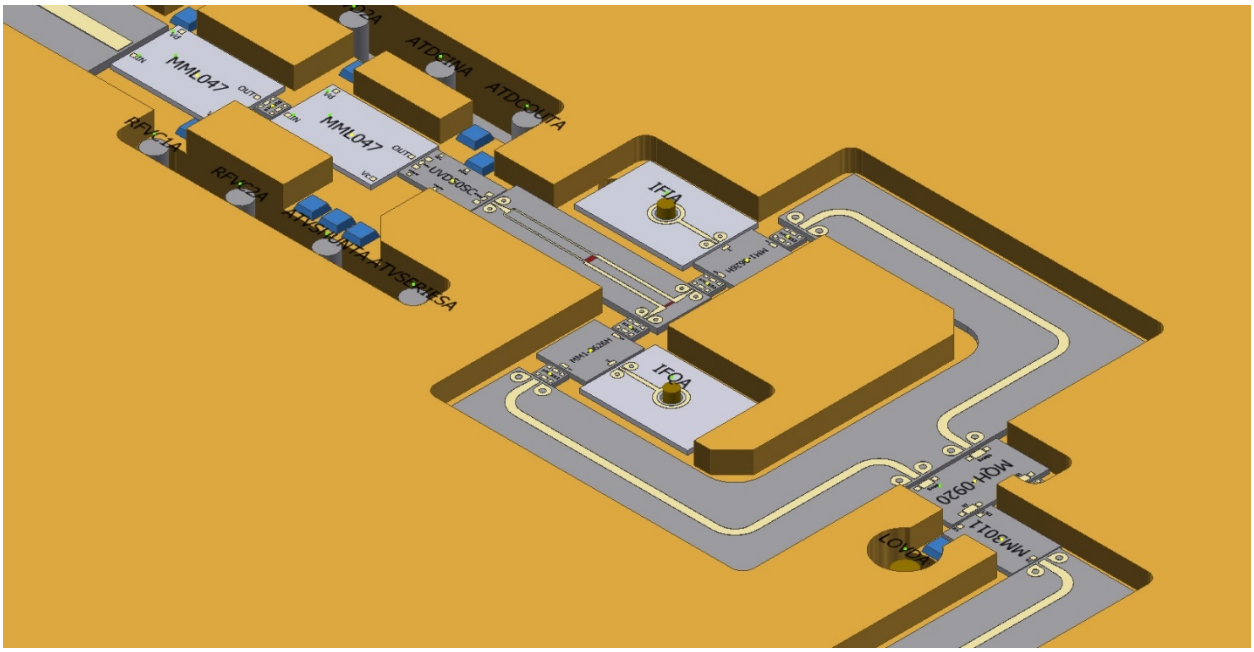


Figure 15. Detail of high-frequency MMICs in the Band 3 IRD module.

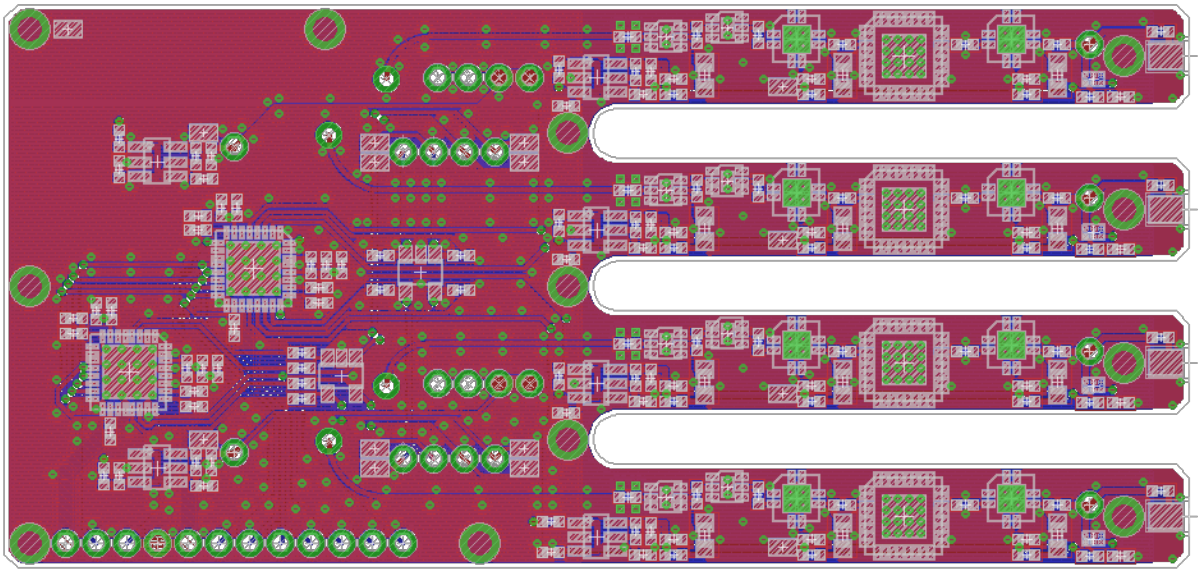


Figure 16. Layout of IF circuit board for Band 3 IRD module.

6.2.2 Direct-Sampled (DS) Receiver Modules

The SADC will directly sampling at baseband for the lowest ngVLA band, Band 1. A conceptual block diagram for such a receiver module is shown in Figure 17. This module includes warm amplification, power leveling, additional amplification, and a final anti-aliasing filter before feeding into the SADC chip and QSFP fiber transceiver. From the SADC forward, the data path is the same as it was for the 2SB modules.

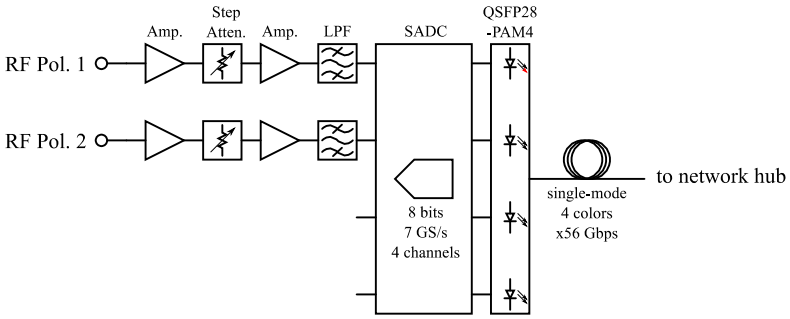


Figure 17 - Block diagram of a direct-sampled (DS) integrated receiver module.

Band 1 will only need two channels (corresponding to the first Nyquist zone for two polarizations) instead of the usual four. Since the commercially available QSFP modules inherently support four lanes, this leaves two lanes unoccupied. The conceptual design has no predetermined use for these lanes.

6.2.3 Other Components

Other subsystem components include the splitters/combiners that interface these modules to the front-end cryogenics, and the internal interconnects between them and the 2SB/DS receiver modules.

6.3 IRD Interfaces with other Subsystems

Interface Control Documents (ICDs) are required between the integrated modules and all connecting systems. The following is a list of ICDs documenting the major interfaces with the IRD subsystem.

Document No.	**Subsys. A**	**Subsystem B**
020.10.40.05.00-0001-ICD_IRD_M&C	IRD	Hardware Interface Layer
020.10.40.05.00-0002-ICD_IRD_DBE	IRD	Digital Backend
020.10.40.05.00-0003-ICD_IRD_ENVIRONMENT	IRD	Environmental Control System
020.10.40.05.00-0004-ICD_IRD_FE	IRD	Front-End
020.10.40.05.00-0005-ICD_IRD_LO	IRD	Antenna Time and Frequency
020.10.40.05.00-0006-ICD_IRD_PWR	IRD	DC Power Supply
020.10.40.05.00-0049-ICD_IRD_BMR	IRD	Bins, Modules, and Racks
020.10.40.05.00-0050-ICD_IRD_AFD	IRD	Antenna Fiber Distribution
020.10.40.05.00-0051-ICD_IRD_MCL	IRD	Monitor and Control System

7 Appendix

7.1 Abbreviations and Acronyms

Acronym	Description
AD	Applicable Document
CDR	Critical Design Review
CoDR	Conceptual Design Review
CW	Continuous Wave (Sine wave of fixed frequency and amplitude)
EIRP	Equivalent Isotropic Radiated Power
EM	Electro-Magnetic
EMC	Electro-Magnetic Compatibility
EMP	Electro-Magnetic Pulse
ENOB	Effective Number of Bits
FDR	Final Design Review
FEA	Finite Element Analysis
FOV	Field of View
FWHM	Full Width Half Max (of Primary Beam Power)
HVAC	Heating, Ventilation & Air Conditioning
ICD	Interface Control Document
IF	Intermediate Frequency
IRD	Integrated Receivers and Digitizers, a.k.a. Integrated Downconverters and Digitizers, etc.
KPP	Key Performance Parameters
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LO	Local Oscillator
LRU	Line Replaceable Unit
MTBF	Mean Time Between Failure
MTTF	Mean Time To Failure
MTTR	Mean Time To Repair
ngVLA	Next Generation VLA
RD	Reference Document
RFI	Radio Frequency Interference
RMS	Root Mean Square
RSS	Root of Sum of Squares
RTP	Round Trip Phase
SAC	Science Advisory Council
SADC	Serial Analog-to-Digital Converter
SINAD	Signal-to-Noise and Distortion ratio
SNR	Signal to Noise Ratio
SRSS	Square Root Sum of the Square
SWG	Science Working Group
TAC	Technical Advisory Council
TBD	To Be Determined
VLA	Jansky Very Large Array