Front End Technical Requirements

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Change Record

Version	Date	Author	Affected Section(s)	Reason
01	2020-04-27	W. Grammer	All	Initial draft version.
02	2020-08-01	W. Grammer	All	Updated draft version.
03	2021-04-01	A. Lear	All	Updated document to include new Reqs template sections; formatting & minor copy-editing.
04	2021-04-27	W. Grammer	All	Added content to new template sections, updated and corrected others.
05	2021-04-29	W. Grammer	All	Edits and updates per input from T. Küsel. Some are still TBD; his comments left in as a placeholder.
06	2021-11-08	W. Grammer	All	Updates and edits from the subsystem review.
A	2021-11-09	A. Lear	All	Formatting, copy edits; prepared PDF for signatures and release.

Table of Contents

1 Introduction

1.1 Purpose

This document presents the complete set of Level 2 subsystem requirements that should guide the design and development of the Front End subsystem. Requirements described in this document are derived from applicable ngVLA System Requirements and system-level specification documents as listed in the Applicable Documents table. The overall requirements hierarchy and management strategy are outlined in [AD01] and [AD02].

The content of these requirements is at the subsystem level, conforming to the system architecture [AD06], but aims to be implementation agnostic within the subsystem boundaries. Some assumptions about the subsystem may be given, but only to the degree necessary to unambiguously define the subsystem requirements.

1.2 Scope

The scope of this document is the ngVLA Front End work package. This consists of the cryogenically cooled receiver assemblies and their associated support electronics, mounted on the ngVLA antenna. It includes interface requirements that must be defined in detail.

It should be noted that the physical extent of the Front End work package extends into other subsystems in some cases: one example is that it includes the displacer cylinder from the cryocooler as part of the cryostat assembly, but not the displacer and motor subassemblies. Other examples of this are detailed later in this document.

This requirements document establishes the performance, functional, design, and test requirements applicable to the ngVLA Front End work package.

2 Related Documents and Drawings

2.1 Applicable Documents

The following documents are applicable to this Technical Specification to the extent specified. In the event of conflict between the documents referenced herein and the content of this Technical Specification, the content of this Technical Specification shall be considered as a superseding requirement.

Ref. No.	Document Title	Rev/Doc. No.
AD01	Systems Engineering Management Plan	020.10.00.00.00-0001-PLA
AD02	Requirements Management Plan	020.10.15.00.00-0001-PLA
AD03	System Requirements	020.10.15.10.00-0003-REQ
AD04	L1 Environmental Specifications	020.10.15.10.00-0001-SPE
AD05	System Electronics Specification	020.10.15.10.00-0008-REQ
AD06	System-Level Architecture Model	020.10.20.00.00-0002-DWG
AD07	Insulation Coordination for Equipment within Low-Voltage Systems	IEC 60664
AD08	Occupational Safety and Health Standards for General Industry	29 CFR Part 1910
AD09	Military Handbook, Reliability Prediction of Electronic Equipment	MIL-HDBK-217F
AD10	Non-Electronic Parts Reliability Data	NPRD-95
AD11	System Technical Budgets	020.10.25.00.00-0002-DSN

Ref. No.	Document Title	Rev/Doc. No.
AD12	Subsystem Reference Design Description for Monitor & Control Hardware Interface Layer	020.30.45.00.00-0004-DSN
AD13	DC Power Supply Reference Design Description	020.30.50.00.00-0002-DSN
AD14	EMC & RFI Mitigation Requirements	020.10.15.10.00-0002-REQ
AD15	L1 Safety Requirements	020.80.00.00.00-0001-REQ
AD25	Antenna Electronics Mass Budgets	020.30.03.00.00-0003-LIS
AD26	Antenna Coordinate Systems	020.10.30.00.00-0001-SPE
AD27	Calibration Requirements	020.22.00.00.00-0001-REQ

2.2 *Applicable ICDs*

The following ICDs define the external boundary of this subsystem and are applicable to its specification:

Ref. No.	Document Title	Rev./Doc. No.
AD16	ICD: Integrated Receiver Downconverter/Digitizer (IRD) to Front End (FED)	020.10.40.05.00-0004-ICD
AD17	ICD: Antenna (ANT) to Antenna Electronics	020.10.40.05.00-0011-ICD
AD18	ICD: Front End (FED) to Cryogenics (CRY)	020.10.40.05.00-0012-ICD
AD19	ICD: Front End (FED) to Monitor and Control Hardware Interface (HIL)	020.10.40.05.00-0015-ICD
AD20	ICD: Front End (FED) to Environmental Control (EEC)	020.10.40.05.00-0017-ICD
AD21	ICD: Front End (FED) to Antenna Time and Frequency References (ATF)	020.10.40.05.00-0016-ICD
AD22	ICD: Front End (FED) to DC Power Supply (PSU)	020.10.40.05.00-0014-ICD
AD23	ICD: Front End (FED) to Bins, Modules and Racks (BMR)	020.10.40.05.00-0040-ICD
AD24	ICD: Front End (FED) to Antenna Fiber Distribution (AFD)	020.10.40.05.00-0041-ICD

2.3 *Reference Documents*

The following references provide supporting context:

Ref. No.	Document Title	Rev/Doc. No.
RD01	ngVLA Science Requirements	020.10.15.05.00-0001-REQ
RD02	W. Grammer, "Front End Reference Design Description", 24 July 2019	020.30.03.00.00-0002-DSN
RD03	W. Grammer, "ngVLA Receiver Cascaded Analysis Tool", May 2021	020.30.05.00.00-0004-GEN
RD04	R. Lehmensiek, W. Grammer, S. Sturgis, "18-Meter Antenna Optics Definition", October 2020	020.25.01.00.00-0006-DSN
RD05	J. Jackson, "ngVLA Antenna Electronics Block Diagram," May 2021	020.30.00.00.00-0005-BLK
RD06	D. Gajewski et. al., "Reliability of GaN/AlGaN HEMT MMIC Technology on 100-mm 4H-SiC," 26th Annual JEDEC ROCS Workshop, Indian Wells, CA, May 2011	N/A
RD07	MTMF/MTBM budget	020.10.25.00.00-0002-DSN
RD08	Electromagnetic Compatibility	IEC 61000-3-5
RD09	T. Küsel, "ngVLA Level I Requirements for Reliability, Availability and Maintainability", February 2021	020.10.50.00.00-0003-MEM

3 Overview of the Front End Subsystem

3.1 Subsystem Boundary, External Interfaces, and Product Breakdown

Figure 1 shows the Front End subsystem boundaries in the context of other systems on the antenna. External systems are shown in boxes with their Configuration Item (CI) number in accordance with the Product Breakdown Structure (PBS) generated from the system architecture model. The ICD document number corresponding to each interface is displayed above the interconnect, where it exists.

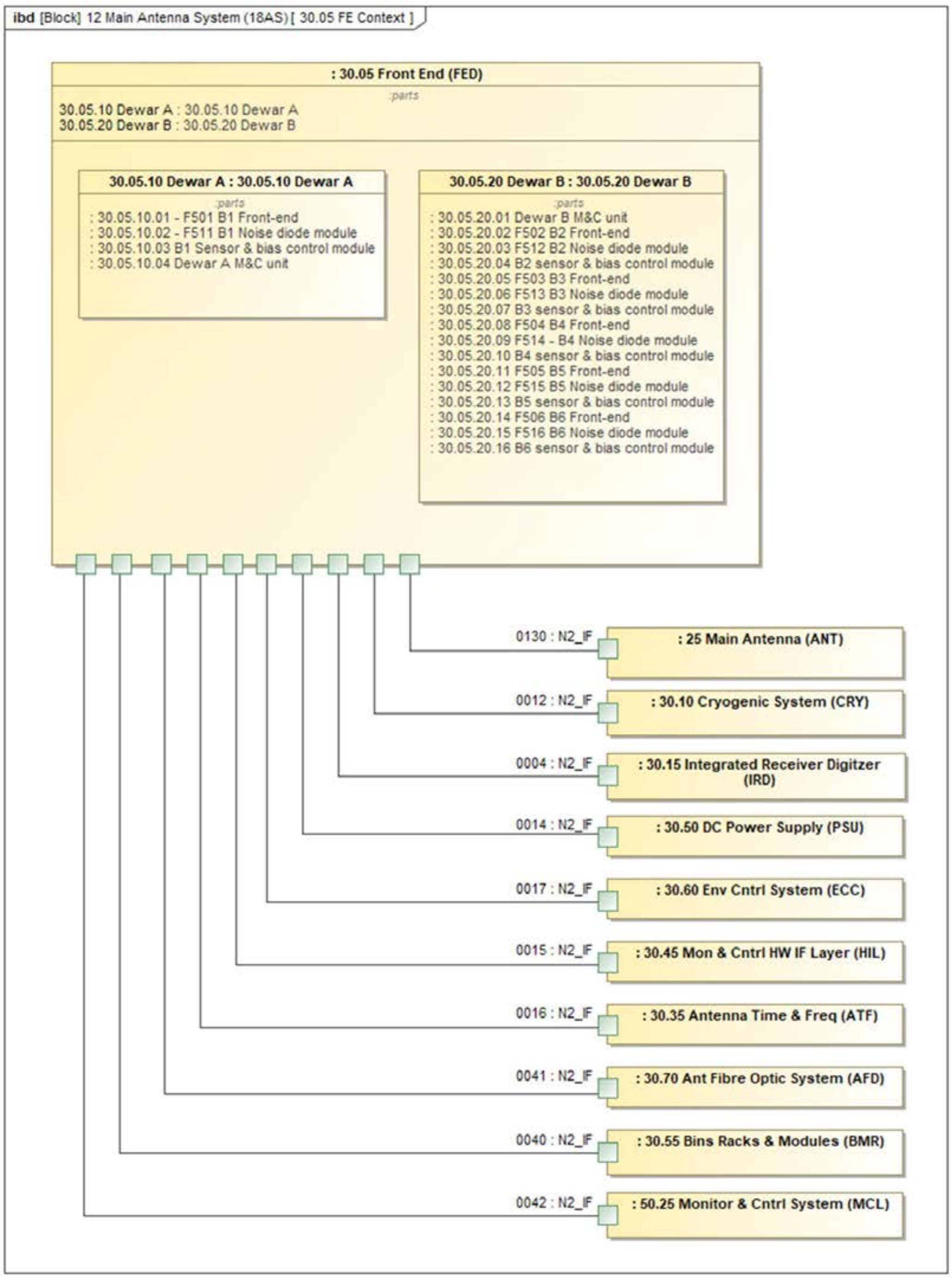

Figure 1: Front End subsystem product breakdown and interfaces with other antenna subsystems.

Figure 1 also shows lower-level products in the Front End subsystem, separated by the cryostat assembly they are associated with. These subassemblies are listed in order by their Configuration Item (CI) number in accordance with the Product Breakdown Structure (PBS) generated from the system architecture model. The next level below these would be at the actual component level, such as LNAs, feed horns, etc.

3.2 Subsystem Functional Overview

The ngVLA Front End subsystem will provide near-continuous frequency coverage from 1.2–116 GHz in multiple receiver bands, with a gap at the atmospheric absorption band between 50.5–70 GHz. The proposed Front End concept [RD02] has six separate cryogenically-cooled, dual linearly-polarized receiver bands, each with an integral feed horn. The upper five bands (2–5) are co-located within a single compact cryostat, while the lowest-frequency band (1) occupies a second cryostat of similar volume and mass. For optimum performance at higher frequencies, waveguide-bandwidth (~1.67:1) receivers are used above 12 GHz, with corrugated feed horns for high aperture efficiency and low spillover. Below 12 GHz, wideband (> 3:1) receivers and feed horns are used to reduce receiver count, total mass, and cost, with modest trades in sensitivity.

Figure 2 shows block diagrams for the six Front End receiver bands. Each receiver produces two orthogonal linearly polarized outputs, either in the feed itself (Bands 1 & 2) or with an external waveguide orthomode transducer (OMT), as on Bands 3–6. There is a single cryogenic low-noise amplifier (LNA) shown per polarization, though the high-frequency bands may require a cascaded second amplifier to produce sufficient overall gain for the external downconverter/digitizer modules. No frequency conversion is performed on any bands in the Front End portion of the system.

Each receiver also contains a calibrated noise injection path ahead of the LNAs for self-calibration during observing. This is shown with a splitter and pair of directional couplers. The noise source driving this path has an adjustable output level (~30 dB dynamic range), located within the cryostat but at ambient temperature.

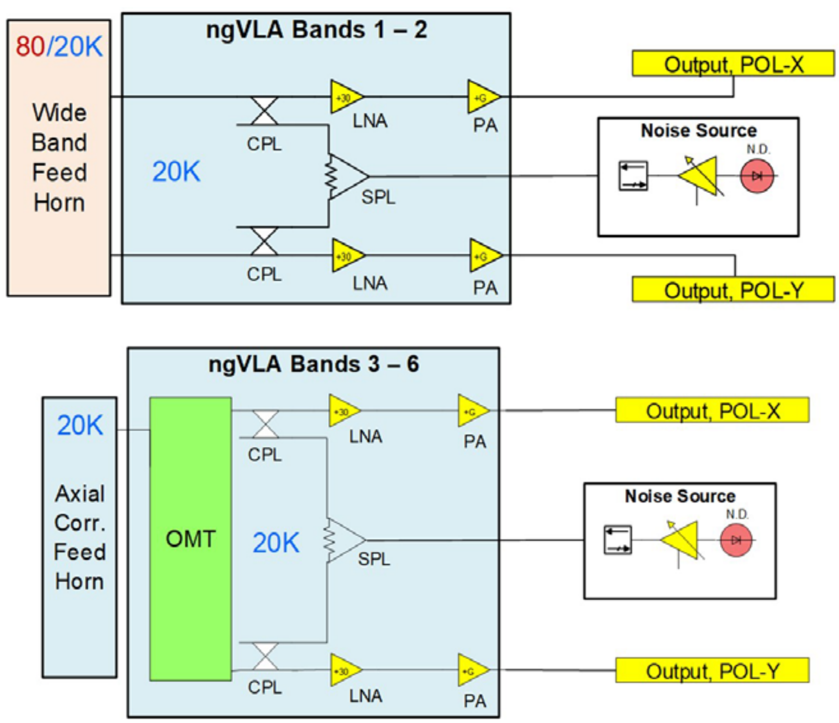

Figure 2: Block diagrams for wideband (Bands 1 & 2) and waveguide-bandwidth (Bands 3–6) receivers.

3.3 Design Driving Requirements

The primary design requirements are to maximize sensitivity for each band while also minimizing the overall operating cost. Therefore, receivers and feeds will be cryogenically cooled, with multiple bands integrated into a common cryostat to the greatest extent possible. Using feed designs that yield broad bandwidths and high aperture efficiencies are key to meeting these goals.

The following tables provides a summary of the major design-driving subsystem requirements. Should there be a conflict between the requirements listed here and the descriptions in Section 7, the latter shall take precedence.

Parameter	Req. #	Value & design driver
Optimum sensitivity	FED0001	Requirement: *Overall sensitivity should be maximized for each band.* Driver: To minimize total # of antennas required for science goals.
Optimum running cost	FED0002	Requirement: *Limit annual maintenance cost to 5% of construction.* Driver: Reduce cryocooler count/antenna to the minimum required, in order to cut power consumption of the cryogenic system.

3.3.1 General Functional Specifications

Parameter	Req. #	Summary of Requirement	Traceability
Frequency Coverage	FED0011	1.2–116 GHz continuous, with a gap between 50.5–70 GHz	SYS0801
Frequency Band Overlap	FED0012	1% minimum, at band edges	SYS0806
Output Polarization Type	FED0013	Dual orthogonal linear	SYS0102
Number of Pixels/Receiver Band	FED0014	One	(TBD)
Number of Receiver Bands	FED0015	Maximum of 6	(TBD)
Number of Cryostats/Cryocoolers	FED0016	Maximum of 2	(TBD)

3.3.2 Other General Requirements

Parameter		Summary of Requirement	Traceability
Mass, Cryostat A	FED0031	49 kg max., excluding cryocooler	[AD25]
Mass, Cryostat B	FED0032	91 kg max., excluding cryocooler	[AD25]
Total Mass Budget for Cryostats	FED0033	140 kg, max., excluding cryocoolers	[AD25]

4 Requirements Management

Derivation of any subsystem requirements shall be included as part of the Front End reference and conceptual design efforts and updated throughout the design. Post CDR/FDR, the subsystem requirements shall only be updated through formal project change control processes, which will include the designer, manufacturer, and NRAO.

4.1 *Requirements Definitions*

Consistent with the Requirements Management Plan [AD03], the following definitions of requirement "levels" are used in the ngVLA program. This requirements document in this document are at the L2 subsystem level.

Requirement Level	Definition
L0	User requirements expressed in terms applicable to their needs or use cases (Science Requirements or Stakeholder Requirements)
L1	Requirements of the System, expressed in technical functional or performance terms (System Level Requirements)
L2	Requirements that define a specification for an element of the system, presuming a system architecture (Subsystem Requirements)

4.2 *Requirements Flow Down*

Figure 3 shows the relationships between the Subsystem (L2) requirements and the System (L1) requirements from which they are derived.

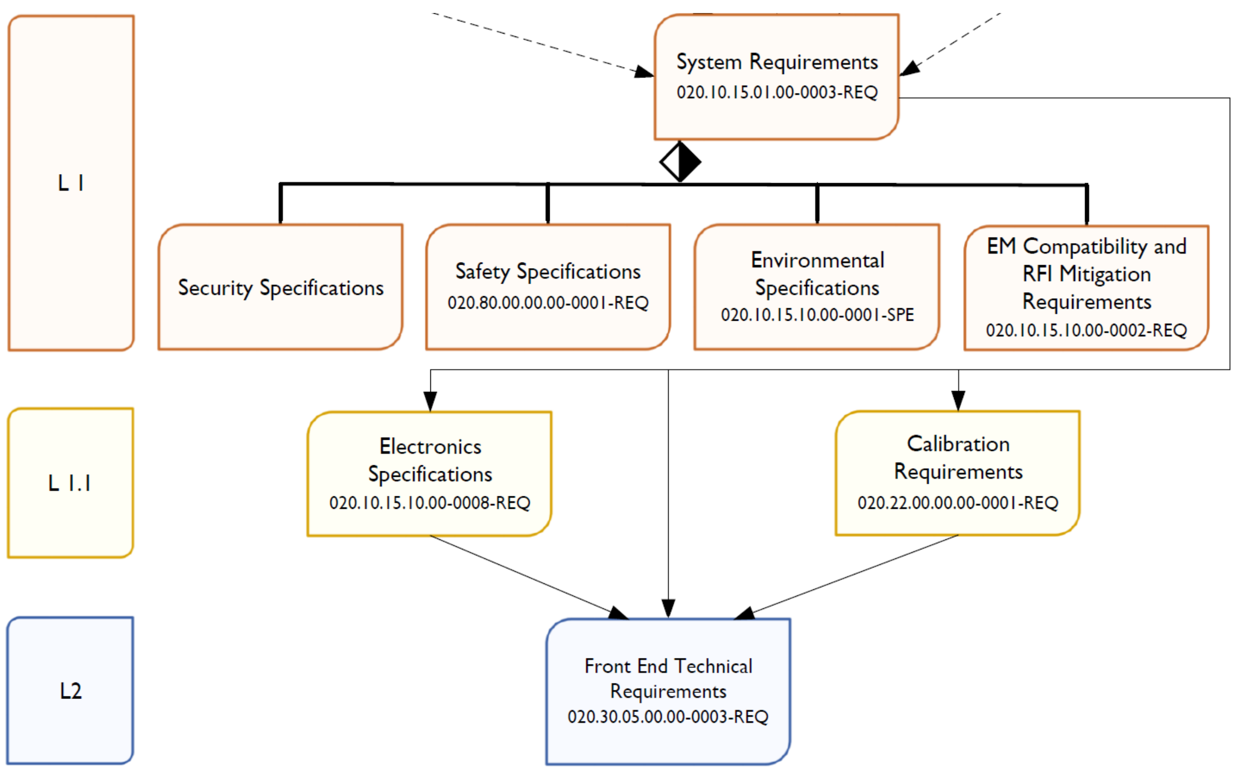

Figure 3: Requirements flow-down to the Front End subsystem requirements.

Individual subsystem specifications (Level 2) flow from the Level 1 requirements, and may not always be directly attributable to a single system requirement. For example, phase drift specifications at the system level may be apportioned to multiple subsystems, or a subsystem spec may be in support of multiple higher-level requirements. Completeness of the Level 2 requirements is assessed at the requirements review of each subsystem.

While this is a top-down design process, the process is still iterative rather than a "waterfall" or linear process. The feasibility and cost of requirements implementation lead to trade-offs that feed back to higher-level requirements. The end goal is to build the most generally capable system that will support the Key Science Goals within the programmatic constraints of cost and schedule. Maintaining enumerated traceability between system requirements and subsystem requirements ensures that this trade-off process can be managed in a controlled way.

4.3 Verb Convention

This document uses "shall" to denote a requirement. The verbs "should" and "must" denote desired but not strictly required parameters. "Will" denotes a future happening. Desired but not required features are noted as "desirable" or "goals."

5 Assumptions

The following assumptions are made in the definition of these subsystem requirements:

- Subsystem requirements apply to performance before any operational calibration corrections are applied unless explicitly stated otherwise.
- Hardware requirements apply to a properly functioning system under the precision operating environmental conditions unless explicitly stated otherwise.
- Hardware requirements assume that all system parts that would normally be in place during observations are working within their respective specifications (e.g., HVAC, RTP system) unless explicitly stated otherwise.

6 Environmental Conditions

The Front End subsystem components will be located on the feed arm of the antenna, in close proximity to the secondary focus of the optic system. This part of the antenna is in an exposed outdoor environment.

6.1 Precision Operating Conditions

The Front End subsystem shall have precision performance as defined in [RD02] under the following outside ambient conditions:

Parameter	Req. #	Value	Traceability
Solar Thermal Load	FED0041	Nighttime only; no solar thermal load within last 2 hours	ENV0311
Wind Speed	FED0042	0 ≤ W ≤ 5 m/s average over 10 mins; 7 m/s peak gusts.	ENV0312
Temperature	FED0043	–15 C ≤ T ≤ +25 C	ENV0313
Temperature Rate of Change	FED0044	< 1.8 °C per hour	ENV0314
Precipitation	FED0045	No precipitation	ENV0315
Precipitable Water Vapor	FED0046	1–6 mm; 4 mm median	ENV0316
Altitude	FED0047	Max. 2500 meters	ENV0351

6.2 Normal Operating Conditions

The Front End subsystem shall have normal performance as defined in [RD01] under the following outside ambient conditions:

Parameter	Req. #	Value	Traceability
Solar Thermal Load	FED0051	Exposed to full sun, 1200W/m^2	ENV0321
Wind Speed	FED0052	W ≤ 7 m/s average over 10 mins; 10 m/s peak gusts.	ENV0322
Temperature	FED0053	–15 C ≤ T ≤ +35 C	ENV0323
Temperature Rate of Change	FED0054	< 3.6 °C per hour	ENV0324
Precipitation	FED0055	No precipitation	ENV0325
Precipitable Water Vapor	FED0056	1–26 mm; 18 mm median	ENV0326

6.3 Limits to the Operating Conditions

The Front End subsystem shall be able to operate for extended periods without sustaining residual damage under the following outside ambient conditions:

Parameter	Req. #	Value	Traceability
Solar Thermal Load	FED0061	Exposed to full sun, 1200W/m^2	ENV0330
Wind Speed	FED0062	W ≤ 15 m/s average over 10 mins; W ≤ 20 m/s gusts	ENV0331
Temperature	FED0063	–20 C ≤ T ≤ +45 C	ENV0332
Precipitation	FED0064	Up to 5 cm/hr over 10 mins	ENV0333
Ice	FED0065	Equivalent to radial ice of 2.5 mm	ENV0334
Relative Humidity	FED0066	0 ≤ RH ≤ 100%; condensation permitted	ENV0335

6.4 *Survival Conditions*

The Front End subsystem when installed on the antenna shall survive without sustaining residual damage the following conditions:

Parameter	Req. #	Value	Traceability
Wind	FED0071	0 m/s ≤ W ≤ 50 m/s average	ENV0341
Temperature	FED0072	–30 C ≤ T ≤ +50 C	ENV0342
Radial Ice	FED0073	2.5 cm	ENV0343
Rain Rate	FED0074	16 cm/hr over 10 mins	ENV0344
Snow Load, Equipment	FED0075	100 kg/m^2 ,horizontal surfaces	ENV0346
Hail Stones	FED0076	2.0 cm	ENV0347

6.5 *Transportation Conditions*

The Front End subsystem LRUs when packaged for transportation shall survive without residual damage the following conditions:

Parameter	Req. #	Value	Traceability
Solar Thermal Load	FED0081	Exposed to full sun, 1200W/m^2	ENV0381
Transportation Temperature	FED0082	–30 C ≤ T ≤ +60 C	ENV0382
General Vibration	FED0083	Vibration on all three axes, for 60 minutes.	ENV0531
Mechanical Shock	FED0084	Drop height of 25 cm, bottom edge or bottom face, up to 5 times	ENV0582

6.6 *Storage Conditions*

The Front End subsystem LRUs shall be stored in an warehouse environment under the following conditions:

Parameter	Req. #	Value	Traceability
Storage Temperature	FED0091	0 C ≤ T ≤ 30 C	ENV0372
Storage Relative Humidity	FED0092	10 ≤ RH ≤ 90%	ENV0373

7 Subsystem Requirements

Derivation of any subsystem requirements shall be included as part of the Front End reference and conceptual design efforts and updated throughout the design. Post CDR/FDR, the subsystem requirements shall only be updated through formal project change control processes, which will include the designer, manufacturer, and NRAO.

7.1 *Functional and Performance Requirements*

These requirements apply to a properly functioning system under the normal operating environmental conditions unless otherwise stated.

7.1.1 RF Frequency Ranges

The specified frequency range is the minimum over which the sensitivity and gain requirements defined for that band are met.

Parameter	Req. #	Value	Traceability
Band 1 Frequency Range	FED0101	1.2–3.5 GHz	SYS0801–0806, SYS0901, IRD0711
Band 2 Frequency Range	FED0102	3.4–12.3 GHz	SYS0801–0806, SYS0901
Band 3 Frequency Range	FED0103	12.3–20.5 GHz	SYS0801–0806, SYS0901
Band 4 Frequency Range	FED0104	20.5–34 GHz	SYS0801–0806, SYS0901
Band 5 Frequency Range	FED0105	30.5–50.5 GHz	SYS0801–0806, SYS0901
Band 6 Frequency Range	FED0106	70–116 GHz	SYS0801–0806, SYS0901

7.1.2 Sensitivity Requirements

Sensitivity of the Front End is quantified by the receiver noise temperature, Trx. It includes all cryogenically cooled RF components in a receiver band (feed horn, OMT, LNAs, etc.), along with the infrared filter(s), vacuum window, and radome cover. A detailed cascaded noise and gain analysis for each receiver band is given in [RD03], and forms a basis for the requirements.

The noise temperatures shall be measured using the Y-factor method, taken at the frequency intervals specified in the table for each band. The average given is an overall unweighted average of all values, across the full band. Maximum limit is typically at the band edges, over a single interval.

Parameter	Req. #	Value	Traceability
Band 1 Noise Temperatures	FED0201	9.7 K average, 11.8 K maximum, 25 MHz meas. interval	SYS1011
Band 2 Noise Temperatures	FED0202	12.1 K, average, 15.1 K maximum, 100 MHz meas. interval	SYS1011–1012
Band 3 Noise Temperatures	FED0203	15.1 K, average, 17.8 K maximum 100 MHz meas. interval	SYS1012
Band 4 Noise Temperatures	FED0204	16.0 K, average, 18.2 K maximum 100 MHz meas. interval	SYS1012
Band 5 Noise Temperatures	FED0205	21.1 K, average, 24.9 K maximum 200 MHz meas. interval	SYS1012
Band 6 Noise Temperatures	FED0206	49.0 K, average, 69.0 K maximum 500 MHz meas. interval	SYS1013

7.1.3 Feed Horn Performance Requirements

Feed horn specifications are derived from electromagnetic and physical optics simulations, and include the antenna optics [RD04]. The Band 1 and 2 feeds are wideband ridged types, while the Band 3–6 feeds are axially corrugated types.

The feed and optics are assumed here to be perfectly aligned on the optical boresight, with no mechanical distortions from gravity, temperature, or wind. Optical surfaces are assumed to be perfectly smooth (i.e., unity Ruze efficiency term), and with negligible conductor loss. Blockage and polarization effects on overall efficiency are also assumed to be negligible in this case.

The sidelobe limits depend on whether they are associated with the main beam (close in), or well away from it (far out). Close-in sidelobes levels are determined by the degree of aperture illumination and edge taper, which in turn are determined by the feed pattern and mapping function used in the optics. Given these were optimized to obtain the highest overall sensitivity (Aeff/Tsys) at 30 GHz, the close-in sidelobe levels are a consequence of this optimization and cannot be specified independently. The far-out sidelobes are primarily a function of the feed horn pattern and may be problematic because they can couple RFI into the signal path.

Cross-polarization limits on the feeds and optics are driven largely by the calibration requirement for polarization leakage stability, which is 0.1% (–30 dB). The feed horn alone is expected to be very stable, even though it may have an absolute cross-polarization level an order of magnitude higher. However, the deformation of the optics with temperature and gravity could have a larger impact on the leakage stability. This is beyond the scope of the Front End subsystem, however.

Parameter	Req. #	Value	Traceability
Beam Subtended Angle, Bands 1–6	FED0301	55 degrees, nom., @ –16 dB edge taper, all planes	ANT0204
Polarizations, Bands 1–6	FED0302	Dual orthogonal linear	CAL0601
Mechanical Alignment, Bands 1–6	FED0303	Respective polarization planes of all antennas within each band shall be aligned within 2° RMS (Goal: 1° RMS) of the nominal antenna focus coordinate plane X and Y axes.	CAL0609, [AD26]
Band 1 Aperture (Illumination) Efficiency	FED0311	0.77 minimum, over 80% of band 0.65 minimum, over the full band	SYS1031–1032
Band 1 Side Lobe Levels	FED0312	0 dBi max., far-out side lobes, all planes	(TBD)
Band 1 Cross Polarization	FED0313	–20 dB max. (Goal: –30 dB), all planes	CAL0604
Band 1 Input Return Loss	FED0314	–15 dB max., both polarizations	(Design)
Band 2 Aperture (Illumination) Efficiency	FED0321	0.92 minimum, over 80% of band 0.90 minimum, over the full band	SYS1031–1032
Band 2 Side Lobe Levels	FED0322	0 dBi max., far-out side lobes, all planes	(TBD)
Band 2 Cross Polarization	FED0323	–20 dB max. (Goal: –30 dB), all planes	CAL0604
Band 2 Input Return Loss	FED0324	–15 dB max., both polarizations	(Design)
Band 3–6 Aperture (Illumination) Efficiency	FED0331	0.94 minimum, over 80% of band 0.92 minimum, over the full band	SYS1031–1032
Band 3–6 Side Lobe Levels	FED0332	0 dBi max., far-out side lobes, all planes	(TBD)
Band 3–6 Cross Polarization	FED0333	–20 dB max. (Goal: –30 dB), all planes	CAL0604
Band 3–6 Return Loss	FED0334	–20 dB max., both polarizations	(Design)

7.1.4 Gain and Bandpass Requirements

The minimum Front End gain requirement stems from a need to reduce noise contributions from subsequent signal amplification and down-conversion stages to <1 K of total system noise temperature.

Gain is specified as between the input of the feed horn and the output connector on the cryostat bulkhead. The gain ripple and slope (flatness) requirements are derived from the system-level requirements of 3 dB and 8 dB, respectively. The system requirement includes contributions from both the Front End and IRD subsystems, but no budget for sharing this allowance across them has been established.

Tentatively, therefore, 20% of the overall budget has been allocated to the Front End. The remaining 80% is allocated to the IRD subsystem, given it has twice as much analog gain and several added lossy signal-conditioning components in its cascade.

Bandpass stability is distinct from gain slope, and can be described as the relative change in the overall bandpass shape. This could be caused by temperature-dependent delay and/or phase angle changes in reflection coefficient on the various cascaded receiver components.

Parameter	Req. #	Value	Traceability
Gain, Bands 1–6	FED0401	30 dB, minimum	SYS1011–1013
Gain Stability, Bands 1–6	FED0402	Normalized gain temperature coefficient < 0.26 dB/K	SYS4901
Gain Ripple, Bands 1–6	FED0403	< 0.6 dB peak-to-peak, on any 100 MHz interval within the central 80% of the band	SYS1702
Gain Slope, Bands 2–6	FED0404	1.6 dB maximum, goal of 1.2 dB, over any 7 GHz interval within the receiver band	SYS1703
Gain Slope, Band 1	FED0405	1.6 dB maximum, goal of 1.2 dB, within the central 80% of the band	SYS1703
Bandpass Stability, Bands 1–6	FED0406	Maximum change < 0.013 dB over 60 minutes	SYS1701
Relative Gain Amplitude Stability Between Polarizations	FED0407	0.3% (0.026 dB) maximum, over 5 minutes	CAL0607

7.1.5 Dynamic Range and Linearity Requirements

Receiver dynamic range is defined as the difference at the receiver output between the system noise on cold sky and the 1 dB compression point, assuming an input of broadband noise with a flat spectral noise characteristic across the full bandwidth of the receiver.

The input power damage threshold is the upper limit of input power, integrated over the full receiver bandwidth, that will not cause permanent damage or destruction of the LNA. The limit is highly dependent on the LNA design, and is thus band specific.

Parameter	Req. #	Value	Traceability
Band 1 Input Dynamic Range	FED0501	46 dB minimum	SYS1203
Band 2 Input Dynamic Range	FED0502	41 dB minimum, 42 dB goal	SYS1203
Band 3 Input Dynamic Range	FED0503	39 dB minimum, 42 dB goal	SYS1203
Band 4 Input Dynamic Range	FED0504	36 dB minimum, 42 dB goal	SYS1203
Band 5 Input Dynamic Range	FED0505	33 dB minimum, 42 dB goal	SYS1203
Band 6 Input Dynamic Range	FED0506	31 dB minimum, 42 dB goal	SYS1203
Band 1 Input Damage Threshold	FED0511	+10 dBm (goal – check if feasible)	SYS1204
Band 2 Input Damage Threshold	FED0512	+10 dBm (goal – check if feasible)	SYS1204
Band 3 Input Damage Threshold	FED0513	+10 dBm (goal – check if feasible)	SYS1204
Band 4 Input Damage Threshold	FED0514	+10 dBm (goal – check if feasible)	SYS1204
Band 5 Input Damage Threshold	FED0515	+10 dBm (goal – check if feasible)	SYS1204
Band 6 Input Damage Threshold	FED0516	+10 dBm (goal – check if feasible)	SYS1204
Gain Calibrator Dynamic Range	FED0550	30 dB	SYS1202

The linearity requirements are specified in terms of the output 1 dB compression point (P1dB), and the system headroom between the noise floor and third order intercept point referred to the input (IIP3). The compression limits are highly dependent on the LNA chosen, and are thus band-specific. The headroom up to the IPT point ensures the desired system linearity in the presence of strong RFI.

Parameter	Req. #	Value	Traceability
Band 1 1dB Compression Point	FED0521	–3 dBm (TBC)	SYS1203
Band 2 1dB Compression Point	FED0522	–10 dBm (TBC)	SYS1203
Band 3 1dB Compression Point	FED0523	–10 dBm (TBC)	SYS1203
Band 4 1dB Compression Point	FED0524	–12 dBm (TBC)	SYS1203
Band 5 1dB Compression Point	FED0525	–15 dBm (TBC)	SYS1203
Band 6 1dB Compression Point	FED0526	–15 dBm (TBC)	SYS1203
Band 1 IP3 Headroom	FED0531	56 dB minimum	SYS1206
Band 2 IP3 Headroom	FED0532	51 dB minimum	SYS1206
Band 3 IP3 Headroom	FED0533	49 dB minimum	SYS1206
Band 4 IP3 Headroom	FED0534	46 dB minimum	SYS1206
Band 5 IP3 Headroom	FED0535	43 dB minimum	SYS1206
Band 6 IP3 Headroom	FED0536	41 dB minimum	SYS1206

7.1.6 Cryogenic Cooling Requirements

To achieve the desired optimum performance from the receivers, cryogenic cooling of the low noise amplifiers (LNAs) and passive components ahead of it is necessary. Theoretically one would want to cool to as low a temperature as possible in order to minimize thermal noise in the receiver chain. In practice, however, cooling to very low temperatures (~4 Kelvin) is more difficult to achieve and maintain, and is also thermodynamically inefficient, which can be costly over the long term. The noise temperature of most LNAs begins to level off below about 20 K, so there's less overall benefit at lower temperatures, particularly if the total RF loss ahead of the LNA is low. Therefore, an upper limit of 20 K for the cooled receiver electronics is specified for both cryostats.

Nearly all cryocoolers used for cooling to this level are two-stage units, with an intermediate-temperature stage between ambient and the low-temperature stage. The intermediate stage is used to cool a radiation shield placed around the cooled receiver(s), and is generally at 50–80 K for the optimum balance of thermal loading between the two stages. Therefore, an upper limit of 80 K for the radiation shield temperature is specified for both cryostats.

Parameter	Req. #	Value	Traceability
Cryostat A 1st Stg. Temperature	FED0601	80 Kelvin, max.	(TBD)
Cryostat A 2st Stg. Temperature	FED0602	20 Kelvin, max.	(TBD)
Cryostat B 1st Stg. Temperature	FED0611	80 Kelvin, max.	(TBD)
Cryostat B 2nd Stg. Temperature	FED0612	20 Kelvin, max.	(TBD)

7.1.7 Monitor and Control Requirements

The expectation with self-monitoring is that the monitor and control system expose lower-level sensors to the monitor and control system when queried. The cadence of access is flexible, and is not expected at high rates (typical access might be on second to minute scales). Any high-cadence monitoring should generally be internal to the Front End control system with a summary output on the interface.

Other features of the M&C interface are to be specified in the Monitor and Control ICD [AD19].

Parameter	Req. #	Value	Traceability
Self-Monitoring	FED0701	The Front End subsystem shall measure, report, and monitor a set of parameters that allow for determination of its status and may help predict or respond to failures.	SYS2601, SYS3101
LRU Alerts	FED0702	An alert shall be generated by a Front End LRU when it detects an abnormal condition or failure, to the extent possible.	SYS3102
High-Cadence Monitoring	FED0703	The Front End subsystem shall be designed to enable a buffered readout mode on selected monitor points with finer time resolution, to support remote engineering diagnostics on Front End LRUs.	SYS3105, SYS2408
LRU Hot Swapping	FED0704	Front End LRUs intended for field replacement shall be hot-swappable by design, and recover with minimal intervention by maintenance and operations staff.	SYS3111
Remote Updates	FED0705	Firmware in embedded processors and configuration data in FPGAs shall be updateable remotely, in situ.	SYS3223
Automatic Configuration on Restart	FED0706	The Front End subsystem shall be capable of reaching an operationally ready Standby state after a full power cycle without human intervention.	SYS3114
Front End Engineering Console	FED0707	The Front End subsystem shall include an engineering console to display status and aid in real-time problem diagnosis.	SYS2407

7.1.8 Spurious Signals/Radio Frequency Interference Generation

The Front End subsystem shall conform to applicable system requirements on self-generated spurious signals, and to applicable EMC and RFI requirements as outlined in [AD14] and [RD08]. Given there is no frequency conversion within any of the Front End receivers, self-generated sources of interference (if present) would likely originate from low-frequency (< 1 GHz) clocking of embedded data acquisition or digital monitor and control electronics. More relevant is the susceptibility of the receivers to in-band emission from nearby subsystems like the IRD, and from external RFI sources.

The limit for a spurious signal at a receiver input is 43 dB below the maximum system noise power over 80% of the band, integrated on a 1 MHz resolution bandwidth.

Parameter	Req. #	Value	Traceability
Band 1 Spurious Signal Input Limit	FED0801	< –168 dBm	SYS2104, SYS1011
Band 2 Spurious Signal Input Limit	FED0802	< –168 dBm	SYS2104, SYS1011, SYS1012
Band 3 Spurious Signal Input Limit	FED0803	< –168 dBm	SYS2104, SYS1012
Band 4 Spurious Signal Input Limit	FED0804	< –167 dBm	SYS2104, SYS1012
Band 5 Spurious Signal Input Limit	FED0805	< –164 dBm	SYS2104, SYS1012
Band 6 Spurious Signal Input Limit	FED0806	< –163 dBm	SYS2104, SYS1013

The other applicable EMC and RFI requirements to the Front End subsystem are listed below. Regarding immunity to supply fluctuations, only those for DC power apply: the Front End subsystem does not use AC power.

Parameter	Req. #	Value	Traceability
Low-Frequency Emissions Limits	FED0821	The spurious emission level at 1 GHz shall not exceed –129 dBm EIRP over a 333 Hz resolution bandwidth, at a distance of 10 meters.	EMC0310
Low-Frequency Emissions Testing	FED0822	Spurious signal emission levels shall be quantified by test over an extended frequency range of 5 MHz to 1 GHz.	EMC0312
Gaseous Discharge Devices	FED0823	No gaseous discharge devices such as cold cathode vacuum gauge sensors shall be used.	EMC0324
Digital Equipment Shielding	FED0824	Circuitry with any digital logic shall be shielded, with any power supply inputs or I/O signals filtered at the chassis bulkhead.	EMC0327
Step Fluctuation Immunity, DC Supply Input	FED0831	Rectangular (step) change of ±12% for up to 3 seconds shall not interrupt normal operation or performance of the electronics.	EMC0412
Short Voltage Dip Immunity, DC Supply Input	FED0832	A 30% drop for up to 10 msec shall cause only temporary loss of function, recovering to normal operation when the disturbance ends.	EMC0423
Long Voltage Dip Immunity, DC Supply Input	FED0833	A 50% drop for up to 100 msec shall cause only temporary loss of function, recovering after remote intervention via the software supervisory system.	EMC0424
Voltage Interruptions, DC Supply Input	FED0834	A drop of 95% or more for a period of 5 seconds shall cause only temporary loss of function, recovering after remote intervention via the software supervisory system.	EMC0432
Transients and Burst Immunity, DC Supply	FED0835	Immunity to transients and bursts shall conform to MIL-STD-461G CS117. The system shall recover to normal operation when the disturbance ends.	EMC0452
Conducted Noise Immunity, DC Supply	FED0836	Immunity to noise shall conform to MIL-STD-461G CS101. The system shall recover to normal operation when the disturbance ends.	EMC0462

7.1.9 Gain Calibrator Requirements

As shown in the preceding block diagrams, each Front End receiver is equipped with a means for injecting a pre-calibrated level of thermal noise into each signal path, using directional couplers and a common noise source. The noise source output can be switched on or off remotely, and the ratio of measured output power in these two states allows the system temperature Tsys to be determined, assuming a known level of injected noise (Tcal) and sufficient gain and bandpass stability over the period of measurement.

Accuracy of the measurement hinges on the stability and repeatability of the noise source output power, both over the timescale of the measurement, and also long term. This implies tight temperature regulation of the noise source and all components in the path up to the injection points that can have significant temperature-dependent gain or loss.

Having a noise source common to both polarizations allows the relative delay between the channels to be determined, by performing a cross-correlation on them. However, this neglects the path length difference ahead of this point (i.e., through the OMT and coupler signal path).

Gain calibrator dynamic range refers to the range of output adjustment required on the noise source used for receiver gain calibration, and is driven largely by the system requirements for solar observing.

Parameter	Req. #	Value	Traceability
Gain Calibrator Output Control	FED0901	On-Off-Switched, remotely set	SYS1801, SYS4801
Gain Calibrator Output Stability	FED0902	< 0.3% drift over 5 minutes < 1% drift over 1 month	CAL0401
Cross-hand Phase Matching	FED0903	Within 10° at upper band edge frequency, between coupler outputs	CAL0608
Gain Calibrator Dynamic Range	FED0904	50 dB	SYS6102

7.1.10 Electrostatic Discharge Immunity and Protection

The Front End subsystem shall conform to applicable system requirements for Electrostatic Discharge (ESD) immunity and protection as outlined in [AD05] and [AD14].

Parameter	Req. #	Value	Traceability
Low-level Air Discharge ESD Immunity	FED1001	Air discharge level up to 8 kV shall not interrupt normal operation or performance. Conformance shall be to MIL-STD-461G CS118.	ETR0501, EMC0471
High-level Air Discharge ESD Immunity	FED1002	Air discharge level up to 15 kV shall cause only temporary loss of function, recovering to normal operation when the disturbance ends. Conformance shall be to MIL-STD-461G CS118.	ETR0505, EMC0472
Direct Contact ESD Immunity	FED1003	Contact discharge level up to 8 kV shall not interrupt normal operation or performance. Conformance shall be to MIL-STD-461G CS118.	ETR0506, EMC0473
ESD Protection for Transport and Storage	FED1004	During shipment, transport, or storage, a cryostat shall be equipped with shorting plugs and conductive caps on all external connections.	ETR0503

7.2 Interface Requirements

In this section, requirements are derived from the applicable ICDs as listed in Section 2.2. As stated in the SEMP [AD01], ICDs define the interface, but do not contain any requirements. All interface requirements that drive the design and verification of the subsystem shall be listed in this section.

7.2.1 Interface to the Power Supply Subsystem (IF 0014)

The Power Supply Subsystem provides DC voltages required by the Front End electronics. Voltages and currents are from the P501 power supply module [AD13].

The electromechanical interface shall consist of a single multi-pin round, twist-lock, or threaded connector interface, of type MIL-DTL-38999. Detailed connector pinout and contact style/sizes, as well as the exact location in the Front End enclosure is still TBD.

Parameter	Req. #	Value	Traceability
Power Supply 1	FED2101	Input voltage: +17.5V ± 10%, regulated Input current: 6A max., limited	ETR0821, ETR0823, ETR0805, [AD22]
Power Supply 2	FED2102	Input voltage: +7.5V ± 10%, regulated Input current: 0.5A max., limited	ETR0821, ETR0823, ETR0805, [AD22]
Power Supply 3	FED2103	Input voltage: –7.5V ± 10%, regulated Input current: 0.1A max., limited	ETR0821, ETR0823, ETR0805, [AD22]
Power Supply 4	FED2104	Input voltage: +5.0V ± 10%, regulated Input current: TBD max., limited	ETR0821, ETR0823, ETR0805, [AD22]

7.2.2 Interface to the Cryogenic Subsystem (IF 0012)

There are three separate interfaces to the cryogenic subsystem. The first is the mechanical interface between the cryostat and cryocooler unit. The second is the thermal load limit on each of the two stages of the cryocooler, in Cryostats A and B. The third is the mechanical interface between the cryostat and vacuum pump line. The subsections that follow detail each one of these interfaces.

7.2.2.1 Cryocooler Mechanical Interface

The cryocooler unit consists of two parts: a drive motor/valve/displacer assembly, and a polished steel cylinder that slides over the displacers. The cylinder is the mechanical interface for both cold stages, and is an integral part of the cryostat assembly. The displacer assembly is external to the cryostat and removable, and is considered part of the cryogenic subsystem. The interface between these parts is an interface plate or flange pattern that allows a gas-tight seal and properly aligns the two parts. Details of the mechanical interface are outlined in the ICD [AD18].

7.2.2.2 Cryostat Thermal Load Limits and Temperature Stability

The thermal loading in Cryostat A and Cryostat B are assumed equal by design, given their similar size and masses. The first stage is used to cool the radiation shield(s) and the Band 1 feed horn in Cryostat A. The second stage is used to cool the remaining feed horns, LNAs, and other receiver RF components.

The gain stability requirement in section 7.1.4 drives a temperature stability requirement for the second stage in both cryostats, primarily because of the temperature coefficient of gain in the LNAs.

Parameter	Req. #	Value	Traceability
Cryostat A 1st Stage Loading	FED2201	20W max., 80 K stage temperature	[AD18]
Cryostat A 2st Stage Loading	FED2202	5W max., 20 K stage temperature	[AD18]
Cryostat A 2nd Stage Temp Stability	FED2203	±0.06 K peak-to-peak, over 200 seconds	SYS4903, SYS4905
Cryostat B 1st Stage Loading	FED2211	20W max., 80 K stage temperature	[AD18]
Cryostat B 2nd Stage Loading	FED2212	5W max., 20 K stage temperature	[AD18]
Cryostat B 2nd Stage Temp Stability	FED2213	±0.06 K peak-to-peak, over 200 seconds	SYS4903, SYS4905

7.2.2.3 Vacuum System Mechanical Interface and Cryostat Leak Rates

Each cryostat has a port for connection to a vacuum pump, located in a separate enclosure on the antenna feed arm. The interface is at an inline coupling flange, which connects the cryostat vessel to a vacuum hose from the pump. Details of the mechanical interface are outlined in the ICD [AD18].

The cryostats will incorporate vacuum sensors and valves, RF windows, and neoprene vacuum seals at vessel joints and interfaces, all of which leak to some extent under vacuum. Atmospheric gas and water vapor leaking into a cooled cryostat will freeze out on the cold surfaces, but over time this will increase thermal loading to a point where the cryocooler has insufficient capacity to maintain stable temperatures on the cold stages. Eventually, the rising temperatures cause accumulated frozen gas within the cryostat to boil off, resulting in a runaway warmup and requiring another pump-down to restore stable cryogenic temperatures. While this would affect overall system availability, a pump-down cycle can be performed remotely, without requiring a visit to the antenna.

The interval between these events can be extended to several years if the overall gas ingress or leak rate is low, in combination with the available cooling margin on the cryocoolers. Quantifying this interval would require some analysis, combined with actual lab testing under controlled conditions. However, the leak rate of individual components can be specified, and the overall total verified by measurement with a leak rate tester in the lab.

Parameter	Req. #	Value	Traceability
Cryostat A Overall Leak Rate	FED2205	$< 10^{-8}$ std. cc He / sec (TBC)	(TBD)
Cryostat A Pumpdown Interval	FED2206	Average of 4 years (TBC), assuming no other equipment or power failures.	(TBD)
Cryostat B Overall Leak Rate	FED2215	$< 10^{-8}$ std. cc He / sec (TBC)	(TBD)
Cryostat B Pumpdown Interval	FED2216	Average of 4 years (TBC), assuming no other equipment or power failures.	(TBD)
Remote Pumpdown of Cryostats	FED2207	The cryostats, vacuum system, and support electronics shall be designed to allow remote, unattended pump-down.	(TBD)

7.2.3 Interface to the Integrated Receivers and Downconverters (IRD) Subsystem (IF 0004)

The IRD subsystem module will be mounted in close proximity to Cryostat B to keep the RF interconnects to it as short as possible. It may be feasible to bolt them directly together, using blind-mate connectors instead of cables/waveguides. Longer armored cables will be used to connect the Band 1 RF outputs of the Cryostat A to the IRD module. Details about the type and number of RF interconnects, as well as their physical locations and mechanical outlines are defined in the ICD [AD16].

The minimum output level from a receiver must be sufficient to reduce the system noise contribution from the IRD to less than 1 K. Based on this and the cascaded gain results in [RD03], the table below shows the minimum required RF output levels from Front End receivers, assuming a fixed (minimum) LNA gain of 30 dB. An antenna elevation of 45 degrees, 1 mm PWV, and cold sky pointing is also assumed. The output spectral power density is integrated over the full nominal bandwidth, assuming a uniform averaged nominal Tsys value for the given band.

Parameter	Req. #	Value	Traceability
Band 1 Output Level	FED2301	–63 dBm, min.	FED0401
Band 2 Output Level	FED2302	–57 dBm, min.	FED0401
Band 3 Output Level	FED2303	–57 dBm, min.	FED0401

Parameter	Req. #	Value	Traceability
Band 4 Output Level	FED2304	–54 dBm, min.	FED0401
Band 5 Output Level	FED2305	–51 dBm, min.	FED0401
Band 6 Output Level	FED2306	–45 dBm, min.	FED0401

7.2.4 Interface to the Antenna Subsystem (IF 0011.1)

A dual offset-Gregorian optical configuration for the antenna is assumed. The key interface specification is the subtended angle of the subreflector at the secondary focal point, which drives the design of all feed horns, and the physical size of the cryostats as well.

Front End cryostat assemblies will be mounted at the secondary focus of the antenna, on a platform attached to the feed arm structure. The platform will include Y-axis and Z-axis motorized positioners for band selection and focusing, respectively, and the temperature-controlled enclosure.

Figure 4 shows a rendering of the mounting concept, which will be the same for both the 18-meter and 6-meter antennas. Detailed mechanical interface drawings are pending completion of the antenna design.

The table below lists the relevant interface parameters between the antenna dish optics and feed horns within the Front End receivers, and the alignment requirements between feed horns and with the Front End enclosure antenna interface plate. Additional interface details are defined in the ICD [AD17].

Note the coordinate axes (X,Y,Z) referred to below are for the antenna focus coordinate plane [AD26].

Parameter	Req. #	Value	Traceability
Feed Subtended Half Angle	FED2401	55° between the optical axis and edge of the subreflector, at the secondary focus	ANT0204
Y-axis Translation Range	FED2402	±0.650 m, along an axis perpendicular to the optical boresight from the secondary mirror	[AD17]
Z-axis Translation Range	FED2403	±0.100 m, along an axis parallel to the optical boresight from the secondary mirror	[AD17]
X-axis Alignment Tolerance	FED2404	±0.25 mm maximum displacement between the feed boresight axis and the optical boresight from the secondary mirror, for each feed selected (i.e., feed phase center translated into the y-z plane).	[AD11]
Feed-to-Feed Boresight Offset, along X-axis	FED2410	All feed boresight axes must like within a ±0.1 mm range along the X-axis	[AD11]
Feed Boresight Angular Tolerance	FED2411	±0.5° (TBC) maximum angular deviation of any feed boresight axis from the enclosure bottom plate, and from a plane perpendicular to the enclosure bottom plane along the direction of the Z-axis	[AD11]

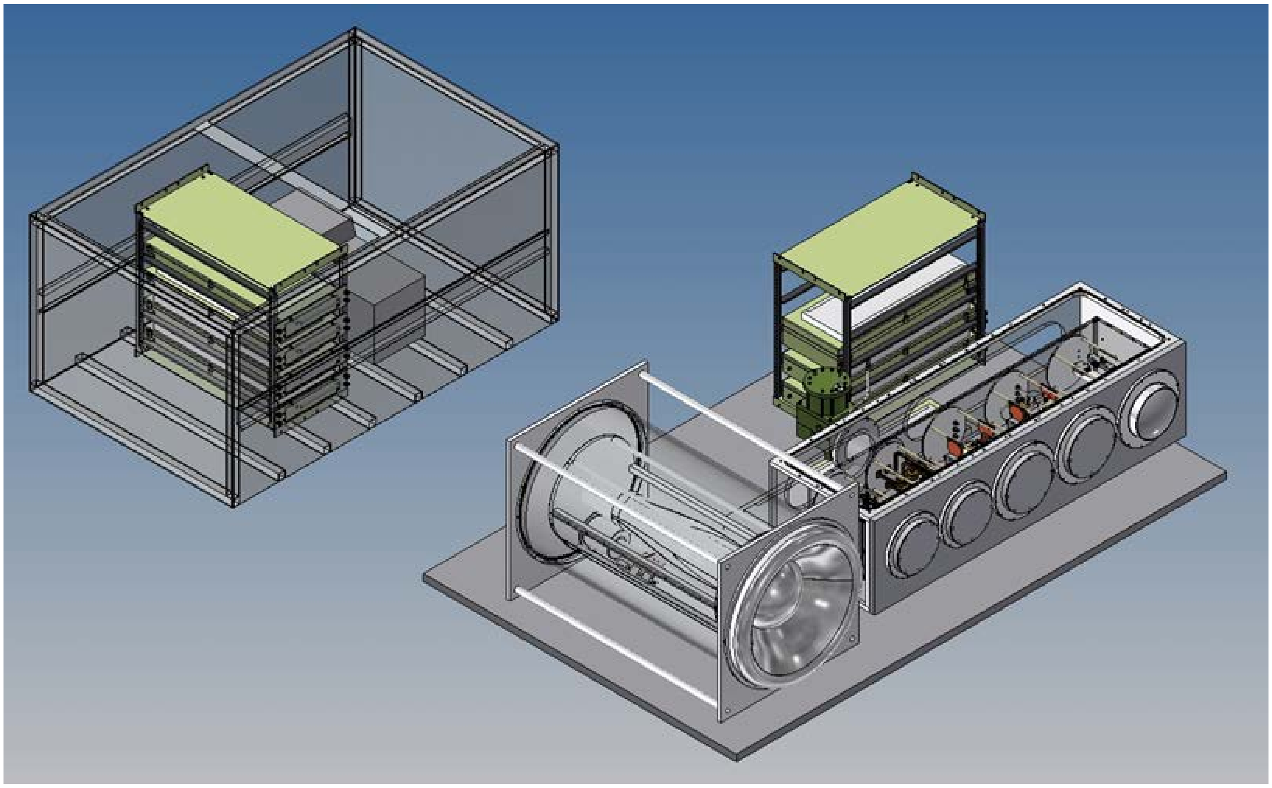

Figure 4: Front End subsystem enclosures, opened to show cryostats, IRD assemblies, and support electronics.

7.2.5 Interface to the Monitor and Control Subsystem (IF 0015)

Nearly all of the support electronics required for each receiver and the cryostat will be integrated into the vacuum space of the respective cryostat to minimize the number of external interface connections required, and to save space and weight by eliminating packaging. The support electronics will provide the following functions [RD05]:

- DC bias/driver circuitry for LNAs, noise calibrator sources, and other active components,
- RF output control/leveling for the noise calibrator sources,
- Input signal conditioning from the cryostat and receiver cartridge temperature sensors, and
- Circuitry for any active temperature control required on the LNAs.

The support electronics are envisioned at present to be implemented on circuit cards, one per receiver band, each soldered directly to a pair of flexible flat ribbon cables (e.g., Kapton/copper) terminated with a Micro-D multipin receptacles. One cable containing the receiver analog I/O signals would plug into a mating connector on the cooled receiver cartridge. The second cable with analog and low-level digital I/O would plug into the corresponding noise calibration source, which would be at ambient temperature.

The hardware interface to each cartridge electronics card will be a synchronous serial I/O multi-drop bus, with separate data and clock inputs. Details of the interface are TBD, but it will likely use some standard form of differential signaling, with all embedded sequential logic externally clocked from the bus to eliminate internal clock oscillators that could cause interference. The communications protocol would include some form of addressing, to allow daisy-chaining of multiple cards onto a single I/O cable. This could possibly include a second redundant port for enhanced reliability.

Electrical connection to the cryostats is assumed to be via multi-conductor shielded cables, with a bulkhead receptacle/cable plug pair at each end. Specific details are undefined at present; however, these will likely consist of single, multi-pin round, twist-locking connector interfaces, with a hermetic glass seal for contacts on the cryostat receptacle side, to maintain vacuum integrity.

Parameter	Req. #	Value	Traceability
(TBD)	FED2501	(TBD)	[AD19]
(TBD)	FED2502	(TBD)	[AD19]

7.2.6 Interface to the Bins, Racks and Modules Subsystem (IF 0040)

Except for the exposed radome and feed horn section on Cryostat A, the Front End subsystem components will be housed entirely within a weather-tight enclosure with temperature regulation. Within this enclosure, the following environmental conditions shall be met:

Parameter	Req. #	Value	Traceability
Temperature (inside)	FED2601	+20° C ≤ T ≤ +30° C	[AD23]
Temperature Rate of Change	FED2602	< 1°C per hour	[AD23]

7.3 Safety

This section defines all design requirements necessary to support the Level-1 Safety, Security, and Cybersecurity requirements derived from [AD04], [AD08], [AD09], and [AD15].

7.3.1 General

In general, the Front End subsystem is fairly benign from a safety standpoint, posing a low risk of injury to personnel or damage to other equipment.

7.3.2 Safety Design Requirements

7.3.2.1 Fire Safety

There are no combustibles, flammable liquids, or gases in the Front End subsystem.

7.3.2.2 Vacuum Safety

Because the cryostats will usually be under vacuum while in storage or transport, there is a potential implosion hazard if one of the large cryostat windows or radomes is breached. The chance of this is low, and it will be minimized by proper design and handling protocols during shipment or installation.

One possible hazard is overpressure in the cryostat during a warmup. Over a long period of operation, gas from the surrounding atmosphere that has leaked through the cryostat windows and seals will freeze out and accumulate on the cold surfaces inside the cryostat. As the cryostat warms after a shutdown, the frozen gas boils off, potentially creating a net positive pressure inside. To prevent damage and potential injuries from sudden rupture of a window in this circumstance, the cryostat shall be equipped with a mechanical overpressure valve to safely bleed off excess positive pressure.

Parameter	Req. #	Value	Traceability
Cryostat Warmup Overpressure	FED3001	A mechanical overpressure relief valve is required for each cryostat, to prevent potential vacuum window rupture during warmup.	SAF0780

7.3.2.3 Mechanical Safety

There are no external exposed moving parts, or known pinch points that could cause injury.

7.3.2.4 Electrical Safety

Electrical equipment installed on the antenna shall comply with their relevant international or US product standard. Electrical installations and equipment shall be specifically built and/or derated in order to safely perform their intended functions under the applicable environmental conditions. Insulation shall be coordinated in conformity with IEC 60664 [AD07] while taking into account the altitude of up to 2500 m above sea level.

7.3.2.5 Handling, Transport, and Storage Safety

The design of the Front End shall incorporate all means necessary to preclude or limit hazards to personnel and equipment during assembly, disassembly, test, and operation. These cryostat radomes and windows are fairly robust but nevertheless must be protected from any impact or abrasion to minimize the chance of breakage and possible injury to personnel from flying debris.

Moderate care must be exercised when removing or installing the Front End cryostat assemblies, as they are heavy, and can be damaged if dropped. A lifting device or small hoist is recommended for installation and removal of the cryostats. Lift points shall be designed into the equipment, and clearly labeled.

Parameter	Req. #	Value	Traceability
Cryostat A Window Protective Cover	FED3011	The cryostat feed horn shall incorporate a removable metallic protective cover, to prevent accidental damage to the window.	ENV0582, ETR1179
Cryostat B Windows Protective Cover	FED3012	The cryostat front plate face shall incorporate a removable metallic protective cover, to prevent accidental damage to the feed windows.	ENV0582, ETR1179
Protective Cover RF Attenuation	FED3013	The protective cover over the feed windows shall provide a minimum attenuation level of TBD dB from in-band RFI, at the receiver input.	SYS1204
Cryostat A Lift Points	FED3021	Engineered lift points shall be designed into Cryostat A to allow safe and balanced removal or installation into the Front End enclosure, using a hoist, chains, and D-rings or hooks.	SAF0250, SAF1050, ETR1178, ETR1191
Cryostat B Lift Points	FED3022	Engineered lift points shall be designed into Cryostat B to allow safe and balanced removal or installation into the Front End enclosure, using a hoist, chains, and D-rings or hooks.	SAF0250, SAF1050, ETR1178, ETR1191

7.4 Reliability, Availability, and Maintainability Requirements

7.4.1 Reliability Availability Maintainability Analysis

A Reliability, Availability, and Maintainability analysis shall be performed to locate weak design points and determine whether the design meets the Maintenance and Reliability requirements. To this end, the Parts Count Method for predicting reliability of the system can be applied, as described in the MIL-HDBK-217F [AD09], but the designer may propose to use other methods. For non-electronic parts, the values of NPRD-95 [AD10] or data from manufacturers or other databases may be used.

Another, more time consuming (and considered more accurate) method, the Parts Stress Analysis Prediction, is also described in [AD09]. This may be used if the result of the Parts Count Method does not comply with the Maintenance and Reliability requirements.

The ngVLA equipment will typically operate at an elevation of 2500 m above sea level, where temperature and pressure might decrease the MTBF relative to that at low elevations. These conditions shall be taken into specific account in the reliability prediction by using the environmental factor given in [AD09]. The analysis shall result in estimates of the Mean Time Between Failures (MTBF) and the Mean Time to Repair (MTTR), assuming that any scheduled preventive maintenance is performed.

The maintenance and reliability requirements support high-level requirements that limit the array's total operating cost. For the antenna electronics system as a whole, approximately half of the MTBF budget for the antenna itself (~17,500 hrs.) is assumed.

The dominant maintenance driver for the antenna electronics is likely to be the cryocooler, as on the VLA. It is estimated to have an MTBF of ~six years, assuming a Gifford-McMahon cooler with a continuous, average running speed of 40 Hz. Given there will be two basically identical cryocoolers per antenna, the net MTBF is therefore three years, which is actually less than what is currently specified for the entire antenna electronic system. However, the actual MTBF in practice will depend on how often the cryocoolers are exchanged during scheduled periodic maintenance. If this is less than three years, the effective MTBF will be longer. This in turn will determine what fraction of the overall antenna electronic system MTBF can be allocated for the Front End and other antenna electronic subsystems.

The intrinsic reliability of the Front End electronics is difficult to estimate due to a lack of reliability data for the cryogenic LNAs under controlled conditions. Life tests of comparable MMIC technology [RD06] indicate the MTBF should be well into the tens of millions of hours. Given the low power and low temperatures inherent in our receivers, intrinsic device reliability would likely be even higher. However, overall LNA reliability will be drastically reduced due to the temperature cycling they are subject to, when a cryocooler needs to be exchanged, or due to a power failure or vacuum loss that causes a warmup. The failure mechanism here is mechanical, usually a broken or loosened bond wire to the MMIC chip. Reliability is again hard to predict, but from the observed failure rate of VLA LNAs, and accounting for a ~3.5-fold reduction in the number of bonds for an equivalent MMIC, the MTBF of the ngVLA Front End with 14 MMIC LNAs works out to roughly 100,000 hours. See the Appendix for details of this analysis.

Vacuum and temperature sensors along with their embedded support electronics should be included in the MTBF/MTTR analysis, but these and other components that can be reasonably deemed to be ancillary to operation may be removed from the determination of compliance with the MTTR and Mean Time Between Maintenance (MTBM) requirements, as defined in [RD09].

"Failure" will be defined as a condition that places the system outside of its performance specifications or into an unsafe state, requiring repair.

Parameter	Req. #	Value	Traceability
Reliability Analysis	FED4001	A Reliability, Availability, and Maintainability analysis shall be performed on the Front End subsystem to locate weak design points and determine whether the design meets the Maintenance and Reliability requirements.	ETR0904
Robustness Analysis	FED4002	Front End electronics shall be subject to a robustness analysis. Results of this analysis are a required part of the design review process.	ETR0905

7.4.2 Reliability Requirements

Parameter	Req. #	Value	Traceability
Front End Subsystem MTTR	FED4003	< 3 hours, with two technicians	SYS2611, SYS3230
Front End Subsystem MTBM	FED4004	8800 hours	SYS2610, [RD07]

7.4.2.1 Maintenance Approach

Required maintenance tasks shall be minimized. Maintenance shall be mainly performed at assembly and subassembly level by exchange of Line Replaceable Units (LRUs). LRUs are defined as units which can be easily exchanged (without extensive calibration, of sufficient low mass and dimension for easiness of handling, etc.) by maintenance staff of technician level.

LRU exchange shall be possible by two trained people within three working hours, on average. It is desirable that LRU replacement be possible using only standard tools identified in a maintenance manual for the Front End. A step-by-step procedure for safe exchange of every LRU shall be provided in the Maintenance Manual.

LRUs shall be defined by the Front End designer, depending on the design. The LRUs will be maintained by the ngVLA project (with or without industrial support).

7.4.2.2 Periodic Preventive Maintenance

Preventive maintenance may be performed at planned intervals to keep the Front End operational and within its specified performance. Any required preventive maintenance should be documented in the Maintenance Manual.

7.5 Configuration Management and Tracking Requirements

The following table lists the configuration management requirements applicable to Front End subsystem LRUs.

Parameter	Req. #	Value	Traceability
Version Control for Software and Firmware	FED5002	All custom software and firmware delivered as part of the Front End subsystem shall be version controlled via a configuration management process.	SYS3602
Configuration Retrieval	FED5003	All configurable Front End LRUs shall retrieve their hardware parameter configuration automatically after installation.	SYS3603
Configuration Monitoring	FED5004	All configurable LRUs shall periodically monitor the System Calibration database for changes, and shall update their configuration based upon a change in relevant parameters.	SYS3604
Physical Tracking	FED7007	A cryostat shall be equipped with a physical tracking label or device (bar code or RFID tag), to allow quick and unique identification.	ETR0402, ETR0405
Remote Identification	FED7008	A cryostat shall identify itself when polled via the M&C network, either directly or through a nearby M&C connected device. Minimum information to be reported includes 1. PBS name and number 2. Serial Number 3. UID and IUID 4. CID Number 5. Hardware Revision Level 6. Firmware Revision Level(s)	ETR0403, ETR0404

7.6 Lifecycle Requirements

Lifecycle costs include manufacturing, transportation, construction/assembly, operation, and decommissioning.

Parameter	Req. #	Value	Traceability
Design Life	FED6001	The Front End shall be designed for an expected operational life of no less than 30 years, commencing from the first delivery to AIV.	SYS2801
Lifecycle Optimization	FED6002	The Front End design shall be designed to minimize total life-cycle costs over the projected design life, extending through system decommissioning/disposal.	SYS2802

7.7 Materials, Parts, and Processes

Parameter	Req. #	Value	Traceability
Metric Fasteners	FED7001	All fasteners shall be metric. An exemption to this are the screws used on standard RF waveguide flanges, which are imperial sizes.	ETR1161
Assembly Hardware	FED7002	Assembly hardware shall conform to requirements listed in Sec. 11.5 of [AD05], where applicable.	ETR1163-1169, ETR1184
Painted Surfaces	FED7003	A suitable paint shall be applied to surfaces with direct and continuous exposure to the outdoor environment. Proper surface preparation shall be done prior to painting, to ensure durability.	ETR1146, ETR1147, ETR1188, ETR1195
Surface Treatment	FED7004	Unpainted and exposed aluminum surfaces shall either be chromated or anodized, depending on if an electrically-conductive surface is required. An exception is any aluminum surface within a cryostat, which will normally be under vacuum.	ETR1143, ETR1145
Cryostat internal surfaces	FED7005	All materials used inside the vacuum space of a cryostat should have a low outgassing rate. Paints, coatings, and surface finishes having the potential for outgassing should be avoided whenever possible.	ETR1192
Cryostat blind cavities	FED7006	Blind tapped holes or isolated cavities need to have outside vents or vented fasteners, to allow trapped air to be efficiently evacuated during pump-down.	ETR1193
Name Plates and Product Marking	FED7007	A cryostat shall be equipped with a durable nameplate which shall be clearly visible in the installed location within the Front End enclosure. The nameplate shall contain the following information: • PBS name and number • Hardware revision level • Serial number • Manufacturing month and year • Unique part number	ETR0401, ETR0409
Weight Labels	FED7008	A cryostat shall have a clearly visible label indicating its weight, both in pounds and kilograms.	ETR0406

Parameter	Req. #	Value	Traceability
Lift and Hoist Point Labels	FED7009	Clearly visible label(s) shall identify the presence and location of all lift or hoist points on a cryostat.	ETR0408
Printed Circuit Boards	FED7010	Printed circuit boards (PCBs) present in any part of the Front End subsystem shall conform to all design requirements listed in Sec. 7 of [AD05].	ETR0701-0717
Component Sources	FED7011	Components shall be sourced from reputable, proven manufacturers, vendors, and/or distributors.	ETR0901
Use of Standard Components	FED7012	Wherever possible, components shall be selected from standard project libraries of parts.	ETR0902
Component Environmental Conditions	FED7013	Electronic and mechanical components shall be used in accordance with their environmental specifications.	ETR0903

7.8 Other Design Requirements

This section covers all other design requirements for Front End subsystem LRUs and assemblies, mainly with the electronics.

7.8.1 DC Power Conditioning, Grounding, and Protection

Parameter	Req. #	Value	Traceability
DC Power Conditioning	FED8101	DC power inputs shall be considered raw power. Internal regulation and filtering is required.	ETR0803
Battery Use	FED8102	Batteries shall not be used within any electronics in the Front End subsystem.	ETR0817
Power Supply Dedicated Returns	FED8103	DC power inputs shall include dedicated current return paths.	ETR0813
Physical Ground Connection	FED8104	A cryostat or LRU chassis/housing shall be electrically connected to the Front End enclosure, using a proper grounding wire.	ETR0804
Supply Returns Separate from Ground	FED8105	Enclosures ties to physical ground, and also signal ground connections, shall never be used as power supply returns.	ETR0814
Supply Voltage Tolerance	FED8106	Electronic modules shall tolerate +/– 10% of the rated voltages.	ETR0823
Thermal Protection	FED8107	All electronics within the Front End subsystem shall be designed to shut down if the ambient temperature is outside the survival range.	ETR0807, FED0072
Thermal Analysis	FED8108	A proper thermal analysis shall be done on all enclosed electronics, to ensure they remain within their specified temperature range when powered.	ETR0816
Transient Protection	FED8109	Transient Voltage Suppression (TVS) devices shall be used on sensitive analog and digital I/O signals and on DC supply inputs entering or exiting LRUs or cryostats.	ETR0818

7.8.2 Programmable Devices and Embedded Firmware

The following requirements shall be applicable to Front End electronic assemblies containing programmable logic devices (FPGAs, CPLDs) or microcontrollers, either as embedded processors or as core modules.

Parameter	Req. #	Value	Traceability
Local Firmware	FED8201	Device firmware shall reside locally and load automatically at power-up, without dependence on a connection to a remote host.	ETR0906
Firmware Updates	FED8202	Device firmware shall be remotely upgradeable **without visiting an antenna**.	ETR0907
Recovery from Lockup	FED8203	Programmable devices shall utilize watchdog timers and power supervisors to recover from lockups. Additionally, remotely commanded hardware resets shall be implemented for these devices.	ETR0908, ETR0909

7.8.3 Indicators and Displays

Parameter	Req. #	Value	Traceability
Power On Indicators	FED8301	All powered LRUs and cryostats shall contain an array of external visual power indicators, one per input voltage. The indicator will be lit when power is applied and in the proper voltage range.	ETR0812, ETR1148-1149, ETR1153
Fault / Warning Indicators	FED8302	All powered LRUs and cryostats that contain visual indicators signaling a fault, warning, or abnormal operation shall conform to the applicable requirements listed from [AD05].	ETR1148, ETR1150, ETR1153
General Status Indicators	FED8303	All powered LRUs and cryostats that contain visual indicators signaling a status condition other than those listed above shall conform to the applicable requirements listed from [AD05].	ETR1148, ETR1152, ETR1153

7.8.4 Electrical Cabling, Wiring, and Connectors

The Front End subsystem will include numerous types of electrical cables, wiring, and connectors. It is critical that the correct types be specified and utilized throughout all parts of the subsystem, and that they be installed and documented in a proper and consistent manner. Specific applicable requirements are shown in the table below.

Parameter	Req. #	Value	Traceability
Electrical Cabling, Wiring	FED8401	The Front End subsystem shall conform to all design requirements listed in Sec. 11.1 of [AD05], where applicable.	ETR1101-1132, ETR1154-1157, ETR1189
Electrical Connectors	FED8402	The Front End subsystem shall conform to all design requirements listed in Sec. 11.2 of [AD05], where applicable.	ETR1133-1142, ETR1158-1160, ETR1185-1187, ETR1197-1199

8 Key Performance Parameters (KPPs)

Key Performance Parameters (KPPs) identify critical subsystem capabilities or characteristics that may either have a detrimental impact on the effectiveness of efficiency of the system if not met, or could have a very large positive impact if the specification is exceeded. Subsystem KPPs typically support System KPPs and there should be traceability between them. Each KPP must have a threshold range and objective value. The responsible engineer designs the subsystem to meet the objective value, but performance within the threshold range is considered acceptable. During the design phase, there should be a concerted effort to optimize the KPPs. If the responsible engineer finds that the minimum threshold level of a KPP cannot be achieved the project office shall be notified immediately.

Key Performance Parameter	Req. #	Traceability L1 Req. #
Band 1 Receiver Noise Temperature Objective value: **9.7 Kelvin** Threshold range: **+2.1 Kelvin**	FED0201	SYS1011
Band 2 Receiver Noise Temperature Objective value: **12.1 Kelvin** Threshold range: **+3.0 Kelvin**	FED0202	SYS1011, SYS1012
Band 3 Receiver Noise Temperature Objective value: **15.1 Kelvin** Threshold range: **+2.7 Kelvin**	FED0203	SYS1012
Band 4 Receiver Noise Temperature Objective value: **16.0 Kelvin** Threshold range: **+2.2 Kelvin**	FED0204	SYS1012
Band 5 Receiver Noise Temperature Objective value: **21.1 Kelvin** Threshold range: **+10.5 Kelvin**	FED0205	SYS1012
Band 6 Receiver Noise Temperature Objective value: **49.0 Kelvin** Threshold range: **+20.0 Kelvin**	FED0206	SYS1013
Band 1 Aperture (Illumination) Efficiency Objective value: **77 %** Threshold range: **–12 %**	FED0311	SYS1031–1032
Band 2 Aperture (Illumination) Efficiency Objective value: **92 %** Threshold range: **–2 %**	FED0321	SYS1031–1032
Band 3–6 Aperture (Illumination) Efficiency Objective value: **94 %** Threshold range: **–2 %**	FED0331	SYS1031–1032

Table 1: Front End Subsystem Key Performance Parameters.

9 Verification

The design will be verified to meet the requirements by analysis (A), inspection (I), demonstration (D), or test (T), each defined below.

Verification by Analysis: The of the subsystem to the requirement is demonstrated by appropriate analysis (hand calculations, finite element analysis, modeling and simulation, etc.).

Verification by Inspection: The compliance of the subsystem to the requirement is determined by a simple inspection of the subsystem or of its design documentation.

Verification by Demonstration: The compliance of the subsystem to the requirement is determined by a demonstration.

Verification by Test: The compliance of the subsystem to the requirement is determined by means of a test with and associated analysis of test data.

Multiple verification methods are allowed over the course of the design phase. The primary (final) verification method to be used for the product during the qualification phase prior to its Critical Design Review is identified below.

9.1 Verification Methods

Req. #	Parameter/Requirement	A	I	D	T
FED0101-0106	Frequency Range, Bands 1–6				X
FED0201-0206	Noise Temperatures, Bands 1–6				X
FED0311, 0321, 0331	Overall Aperture Efficiency	X		X	
FED0312-0313, FED0322-0323, FED0332-0333	Feed Horn Radiation Pattern	X		X	
FED0314, 0324, 0334	Feed Horn Return Loss				X
FED0401	Gain, Bands 1–6				X
FED0402	Gain Stability, Bands 1–6				X
FED2201-2212	Cryocooler Thermal Loading	X		X	
FED4001	Front End Subsystem MTBF	X		X	
FED5001	Design Life			X	

9.2 Verification Requirements

[This section defines how requirements will be verified during the qualification phase, leading up to CDR. Generally, all requirements that are verified by Analysis or Testing should have a corresponding Verification Requirement listed in this section. Examples are: (a) specifying FEA load conditions for verifying a mechanical part through analysis; (b) conditions and methods for testing the performance of a prototype in the lab.]

Req. #	Parameter/ Requirement	Verification Requirement

10 Appendix

10.1 Abbreviations and Acronyms

Acronym	Description
AC	Alternating Current
AD	Applicable Document
AIV	Acceptance, Integration, and Verification
CAD	Computer Aided Design
CI	Configuration Item
CDR	Critical Design Review
CoDR	Conceptual Design Review
CPLD	Complex Programmable Logic Device
DC	Direct Current
EMC	Electro-Magnetic Compatibility
FDR	Final Design Review
FPGA	Field Programmable Gate Array
IPT	Integrated Product Team
I/F	Interface
I/O	Input/Output
ICD	Interface Control Document
IPT	Integrated Product Team
IRD	Integrated Receiver Downconverter/Digitizer
KPP	Key Performance Parameter
LNA	Low Noise Amplifier
LRU	Line Replaceable Unit
MMIC	Monolithic Microwave Integrated Circuit
MOE	Measure of Effectiveness
MOP	Measure of Performance
MTBF	Mean Time Between Failure
MTBM	Mean Time Between Maintenance
MTTR	Mean Time To Repair
M&C, M/C	Monitor and Control
ngVLA	Next Generation Very Large Array
NRAO	National Radio Astronomy Observatory
PBS	Product Breakdown Structure
PWV	Precipitable Water Vapor
RD	Reference Document
RFI	Radio Frequency Interference
TBC	To Be Confirmed
TBD	To Be Determined
TPM	Technical Performance Measure
VLA	Jansky Very Large Array

10.2 MTBF Estimation for ngVLA Front End

1. EVLA LNA Failure Rate, from March 2013 to September 2018 (5.5 years)

Year	# repairs*
2013	10
2014	6
2015	17
2016	6
2017	10
2018	5
TOTAL:	**54**

* Excludes LED failures, upgrades

Active Antennas:	**27**
Cryo LNAs per antenna:	**16**
Total LNAs:	**432**
Duration (yrs):	**5.5**
Duration (hrs):	**48,213**

Failure Rate (/hr-LNA):	**2.593E-06**
MTBF (hrs):	**3.857E+05**

2. Predicted ngVLA MMIC LNA MTBF (1 antenna):

Failure reduction factor:	**3.6**	(relative wire bond count)
MMIC LNAs per antenna:	**14**	(2 ea, Bands 1–5; 4 on Band 6)

Failure Rate (/hr-Ant):	**1.008E-05**
MTBF (hr-Ant):	**9.918E+04**

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