



Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B



Central Signal Processor Requirements Specification

020.40.00.00.00-0001-REQ

Status: **RELEASED**

PREPARED BY	ORGANIZATION	DATE
O. Yeste Ojeda	CDL, NRAO	2022-02-04
W. Shillue	CDL, NRAO	

APPROVALS	ORGANIZATION	SIGNATURES
W. Shillue, CSP & Timing IPT Lead	Project Office, ngVLA/NRAO	<u><i>William Shillue</i></u> William Shillue (Feb 11, 2022 08:37 EST)
R. Selina, Project Engineer	Project Engineer Dept., ngVLA/NRAO	<u><i>R. Selina</i></u> R. Selina (Feb 11, 2022 08:33 MST)
T. Kusel, System Engineer	Systems Dept., ngVLA/NRAO	<u><i>Thomas Kusel</i></u> Thomas Kusel (Feb 11, 2022 12:07 EST)
W. Esterhuyse, Antenna Project Manager	Project Office, ngVLA/NRAO	<u><i>W. Esterhuyse</i></u>

RELEASED BY	ORGANIZATION	SIGNATURES
W. Esterhuyse, Antenna Project Manager	Project Office, ngVLA/NRAO	<u><i>W. Esterhuyse</i></u>



Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

Change Record

Version	Date	Author	Affected Section(s)	Reason
A	2019-12-31	A. Lear	All	Incorporated minor edits by M. McKinnon. Prepared PDF for approvals and release. Reference Design Release.
A.01	2021-08-09	O. Yeste Ojeda	All	Major revision based on 020.10.10.20.00-0005 "Subsystem Requirements Specification template" and 020.40.00.00.00-0001-REQ-A "Central Signal Processor: Preliminary Technical Requirements."
A.02	2021-08-25	O. Yeste Ojeda	All	Incorporated minor edits by R. Selina.
A.03	2021-09-30	O. Yeste Ojeda	All	Minor edits. Added CSPI030. Populated Section 9.
A.04	2022-02-04	O. Yeste Ojeda	All	Revision based on feedback from internal review.
B	2022-02-10	A. Lear	All	Formatting, copy-edits; prepared PDF for signatures and release.



Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

Table of Contents

1	Introduction.....	5
1.1	<i>Purpose.....</i>	5
1.2	<i>Scope.....</i>	5
2	Related Documents and Drawings.....	6
2.1	<i>Applicable Documents.....</i>	6
2.2	<i>Applicable ICDs.....</i>	6
2.3	<i>Reference Documents.....</i>	7
3	Overview of Subsystem.....	7
3.1	<i>Subsystem Boundary, Context, and External Interfaces.....</i>	7
3.2	<i>Subsystem Product Breakdown.....</i>	9
3.3	<i>Subsystem Functional Overview.....</i>	10
3.4	<i>Design Driving Requirements.....</i>	16
4	Requirements Management.....	17
4.1	<i>Requirements Definitions.....</i>	17
4.2	<i>Requirements Flow Down.....</i>	17
4.3	<i>Verb Convention.....</i>	18
5	Assumptions.....	18
6	Environmental Conditions.....	19
6.1	<i>Normal Operating Conditions.....</i>	19
6.2	<i>Transportation Conditions.....</i>	19
6.3	<i>Storage Conditions.....</i>	19
6.4	<i>Site Elevation.....</i>	19
6.5	<i>Environmental Protection Requirements.....</i>	20
6.5.1	<i>Seismic.....</i>	20
6.5.2	<i>Vibration.....</i>	20
6.5.3	<i>Mechanical Shock.....</i>	20
6.5.4	<i>Lightning, Dust, Fauna, Solar Radiation, Rain/Water Infiltration, & Corrosion Protection.....</i>	20
7	Subsystem Requirements.....	21
7.1	Functional and Performance Requirements.....	21
7.1.1	<i>Operating Mode Requirements.....</i>	21
7.1.2	<i>General Functional and Performance Requirements.....</i>	22
7.1.3	<i>Subarray Operation Requirements.....</i>	23
7.1.4	<i>Interferometric Requirements.....</i>	25
7.1.5	<i>Beamforming Requirements.....</i>	26
7.1.6	<i>Transient Analysis Requirements.....</i>	27
7.1.7	<i>Sideband Separation Requirements.....</i>	28
7.1.8	<i>Sub-Band Generation Requirements.....</i>	28
7.1.9	<i>RFI Mitigation Requirements.....</i>	29
7.1.10	<i>Delay and Phase Tracking Requirements.....</i>	29
7.1.11	<i>Dedispersion Requirements.....</i>	30
7.1.12	<i>Folding Requirements.....</i>	30
7.2	Interface Requirements.....	30
7.2.1	<i>020.10.40.05.00-0002 IRD–DBE Interface Requirements.....</i>	30
7.2.2	<i>020.10.40.05.00-0006 Power Supply–DBE Interface Requirements.....</i>	31
7.2.3	<i>020.10.40.05.00-0040 Antenna Bins, Modules, and Racks–DBE Interface Requirements.....</i>	32



Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

7.2.4	020.10.40.05.00-0076 DBE–MCL System Interface Requirements.....	33
7.2.5	020.10.40.05.00-0041 Antenna Fiber Distribution Interface Requirements.....	33
7.2.6	020.10.40.05.00-0095 ngVLA Site Buildings Interface Requirements.....	33
7.2.7	020.10.40.05.00-0105 CSP–MCL System Interface Requirements	34
7.2.8	020.10.40.05.00-0114 CSP–Online Subsystem Interface Requirements	35
7.2.9	020.10.40.05.00-0119 CSP–Central Fiber Infrastructure Interface Requirements	35
7.2.10	020.10.40.05.00-0122 DBE–Antenna Time and Frequency Interface Requirements	36
7.2.11	020.10.40.05.00-0123 CSP–LO Reference & Timing Generation Interface Requirements ...	36
7.3	Safety and Security Requirements.....	36
7.4	Reliability, Availability, and Maintainability Requirements.....	37
7.5	Configuration and Document Management Requirements.....	39
7.6	Life Cycle Requirements.....	39
8	Key Performance Parameters (KPPs)	41
9	Verification	42
9.1	Verification Methods	42
9.1.1	Functional and Performance Requirements	42
9.1.2	Interface Requirements	43
9.1.3	Safety and Security Requirements	44
9.1.4	Reliability, Availability, and Maintainability Requirements	45
9.1.5	Configuration and Document Management Requirements	45
9.1.6	Life Cycle Requirements	45
9.1.7	Environmental Requirements.....	46
9.2	Verification Requirements	46
10	Appendix.....	48
10.1	Abbreviations and Acronyms.....	48



Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

I Introduction

1.1 Purpose

This document presents the complete set of Level 2 subsystem requirements that guide the design and development of the Central Signal Processor (CSP) subsystem. Requirements described in this document are derived from applicable ngVLA System Requirements and System-Level Specification documents as listed in the Applicable Documents table. The engineering process and requirements hierarchy that govern this specification are defined in [AD01] and [AD02] respectively.

The content of these requirements is at the subsystem level, conforming to the system architecture [AD06], but aims to be implementation agnostic within the subsystem boundaries. Some assumptions about the subsystem may be given, but only to the degree necessary to unambiguously define the subsystem requirements.

1.2 Scope

The scope of this document is the specification of the Central Signal Processor Subsystem, configuration item number 020.40.00.00.00, which includes the antenna Digital Back End, configuration number 020.30.25.00.00, of the ngVLA system. The scope includes

- Assumptions on which the requirements are based.
- Definition of environmental conditions to be used in the definition of requirements.
- A complete set of requirements for the subsystem needed for the development, operation and maintenance of the subsystem, including interface requirements that are derived from the applicable list of ICDs.
- Numbering of all requirement and establishment of traceability to higher level requirements.
- Verification requirements and their traceability to the subsystem main requirements.
- Identification of Key Performance Parameters (KPPs) at the subsystem level.

The Level 2 Subsystem Requirements, along with detailed explanatory notes, are found in Section 7. The notes contain elaborations regarding the meaning, intent, and scope of the requirements. These notes form an important part of the definition of the requirement. In many cases, the notes contain an analysis of how the numeric values of requirements were derived to ensure correct interpretation of the requirements and to resolve ambiguity.

In cases where the requirements analysis is incomplete, such values are marked with TBD or TBC, which need to be resolved before the final specification is published.



Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

2 Related Documents and Drawings

2.1 Applicable Documents

The following documents apply to this Requirements Specification to the extent specified. In the event of a conflict between the documents referenced herein and the content of this Requirements Specification, the content of the highest-level specification (in the requirements flow-down) shall be considered the superseding requirement for design elaboration and verification.

Ref. No.	Document Title	Rev./Doc. No.
AD01	ngVLA Systems Engineering Management Plan	020.10.00.00.00-0001-PLA
AD02	ngVLA Requirements Management Plan	020.10.15.00.00-0001-PLA
AD03	ngVLA System Requirements	020.10.15.10.00-0003-REQ
AD04	LI System Environmental Specifications	020.10.15.10.00-0001-SPE
AD05	LI System EMI/RFI Requirements	020.10.15.10.00-0002-REQ
AD06	System-Level Architecture Model	020.10.20.00.00-0002-DWG
AD07	LI Safety Specification	020.80.00.00.00-0001-REQ
AD08	Security Plan and Requirements	020.80.00.00.00-0003-REQ
AD09	ngVLA System Electronics Specifications	020.10.15.10.00-0008-REQ
AD10	LI System Technical Budgets	020.10.25.00.00-0002-DSN

2.2 Applicable ICDs

The following ICDs define the external boundary of this subsystem and are applicable to its specification:

Ref. No.	Document Title	Rev./Doc. No.
AD20	Integrated Receivers & Digitizers–Digital Back End Interface Specification	020.10.40.05.00-0002-ICD
AD21	Power Supply–Antenna Electronics Interface Specification	020.10.40.05.00-0006-ICD
AD22	Antenna Bins, Modules, & Racks–Antenna Electronics Interface Specification	020.10.40.05.00-0040-ICD
AD23	Digital Back End–Monitor & Control System Interface Specification	020.10.40.05.00-0076-ICD
AD24	Antenna Fiber Distribution Interface Specification	020.10.40.05.00-0041-ICD
AD25	ngVLA Site Buildings Interface Specification	020.10.40.05.00-0095-ICD
AD26	CSP–Monitor & Control System Interface Specification	020.10.40.05.00-0105-ICD
AD27	CSP–Online Subsystem Interface Specification	020.10.40.05.00-0114-ICD
AD28	CSP–Central Fiber Infrastructure Interface Specification	020.10.40.05.00-0119-ICD
AD29	Digital Back End–LO Reference & Timing Interface Specification	020.10.40.05.00-0122-ICD
AD30	Central Signal Processor–LO Reference & Timing Interface Specification	020.10.40.05.00-0123-ICD

Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

2.3 Reference Documents

The following documents are referenced within this text or provide supporting context:

Ref. No.	Document Title	Rev./Doc. No.
RD01	Central Signal Processor Design Description	020.40.00.00.00-0005-DSN
RD02	ngVLA Time-Domain Correlator Considerations	P. Demorest, 01/05/18.
RD03	Interferometry and Synthesis in Radio Astronomy, 3 rd Ed.	A. R. Thompson, J. M. Moran, G. W. Swenson Jr., 2017.
RD04	ALMA Memo No. 452, Passband Shape Deviation Limits	L. R. D’Addario, 04/09/03.

3 Overview of Subsystem

3.1 Subsystem Boundary, Context, and External Interfaces

The Central Signal Processor (CSP) is a heterogeneous subsystem consisting of various digital signal-processing sub-elements that, together, convert the digitized voltage from each active receiver at the antenna into raw data products, such as uncalibrated visibilities, average pulse profiles, or beamformed digital voltage for data recorders. All signal processing within the CSP is digital and real-time, two characteristics that help determine its boundary¹.

Most of the CSP equipment is located at the correlator building within the ngVLA Site Buildings subsystem (NSB, CI number 020.61.10.00.00). Figure 1 graphically represents the product context of the CSP housed in the central processing building, i.e., the Sub-Band Processor (SBP), the Pulsar Engine (PSE), and the CSP Switched Fabric (CSF). As seen in the figure, the DBE is treated in this regard as an independent subsystem because its location in the antenna pedestal results in a different product context.

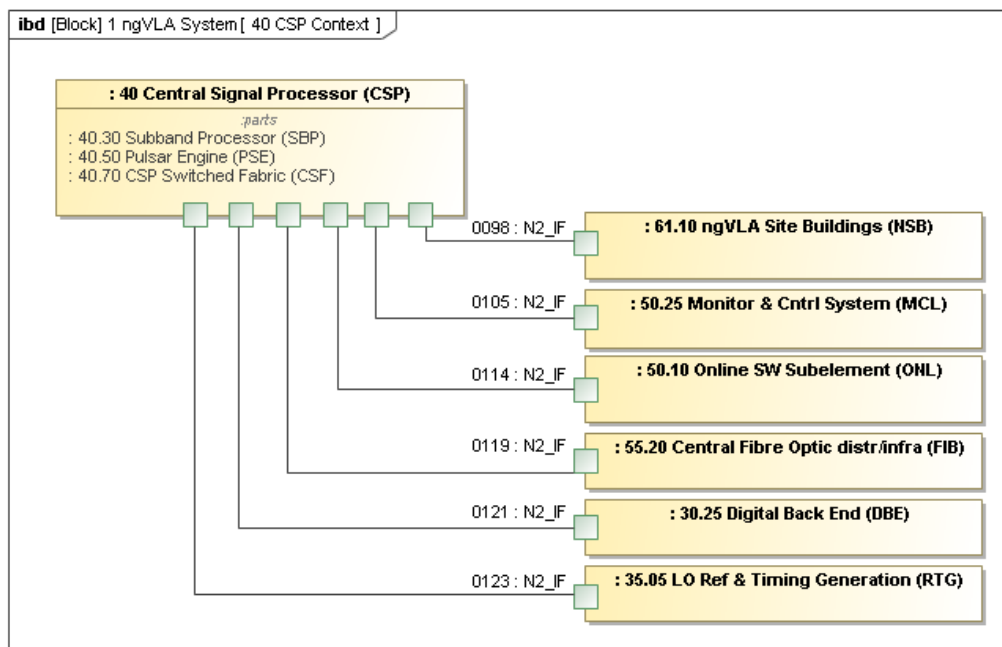


Figure 1: Central Signal Processor product context.

¹ That does not mean, however, that all real-time digital signal processing is done by the CSP.

Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

The product context of the DBE is shown next in Figure 2. The NSB subsystem provides the CSP with power, HVAC room cooling, physical space, and RFI shielding [AD25]. The current CSP concept includes a distributed sub-element located at each antenna site, known as the Digital Back End (DBE, CI number 020.30.25.00.00). Migration of this system to the correlator building for the closest antenna sites is an option yet under study. At the antenna, the Bins, Modules, & Racks sub-element (BMR, CI number 020.30.55.00.00) must provide the DBE with room, cooling, and RFI shielding [AD22], while the DC Power Supply sub-element (PSU, CI number 020.30.50.00.00) provides it with power [AD21].

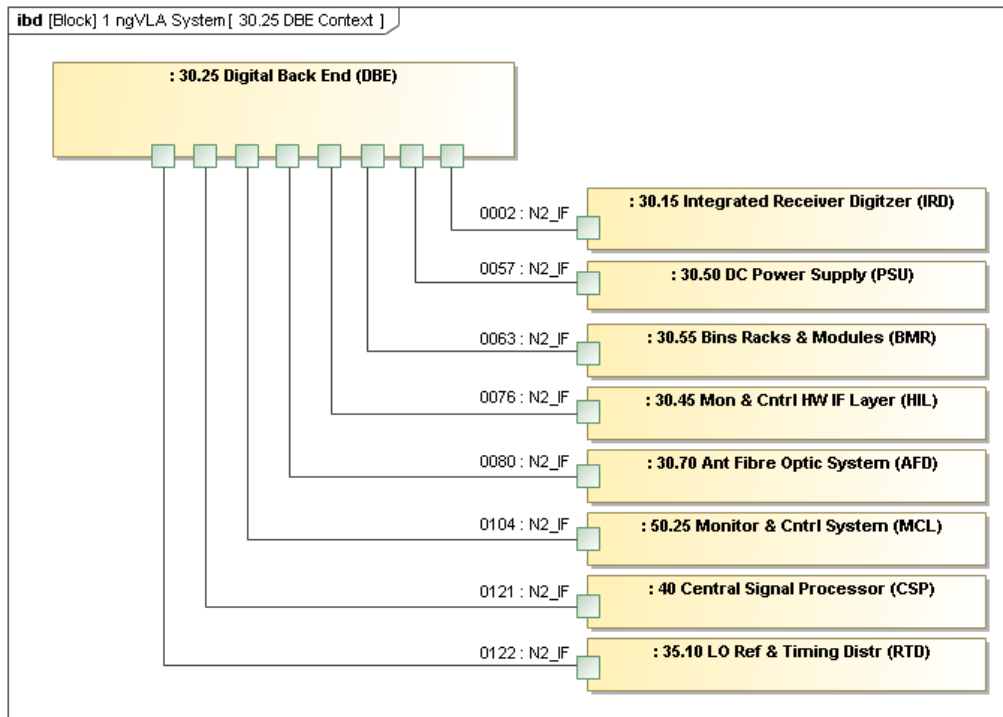


Figure 2: Digital Back End product context.

Data digitized at the antenna stations must be transmitted to the correlator building. When the DBE is located at the antenna site, data are transmitted through an interface between the DBE and the Antenna Fiber Optic subsystem (AFD, CI number 020.30.70.00.00) as per [AD24]. At the correlator building, data from the antenna sites is received through an interface between the CSP and the Central Fiber Optic Distribution subsystem (FIB, CI number 020.55.20.00.00) [AD28]. This interface may connect to the DBE and the CSP Switched Fabric (CSF, CI number 020.40.70.00.00) sub-element of the CSP depending on the DBE location at the correlator building or the antenna site, respectively. In general, data transmitted from the DBE at the antenna is delivered to other CSP sub-elements in the central building by the AFD and the FIB subsystems.

Any time and frequency references needed by the CSP are obtained from its interfaces with the LO Reference and Timing Generation subsystem (RTG, CI number 020.35.05.00.00) [AD30] and the LO Reference and Timing Distribution subsystem (RTD, CI number 020.35.10.00.00) for its DBE sub-element [AD29].

Data products generated by the CSP are sent to the Computing and Software System (CSS, CI number 020.50.00.00.00), specifically its Online sub-element (ONL, CI number 020.50.10.00.00) [AD27]. The Monitoring & Control sub-element (MCL, CI number 020.50.25.00.00) of the CSS also interfaces with the CSP at various levels [AD23, AD26].

Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

Finally, regardless of the DBE location, the CSP interfaces with the Integrated Receiver Digitizer (IRD, CI number 020.30.15.00.00), which generates the digitized data to be processed [AD20].

3.2 Subsystem Product Breakdown

The CSP is composed of three sub-elements performing DSP tasks, i.e., the Digital Back End (DBE, CI number 020.30.25.00.00), the Sub-band Processor (SBP, CI number 020.40.30.00.00), and the Pulsar Engine (PSE, CI number 020.40.50.00.00); along with the CSP Switched Fabric (CSF, CI number 020.40.70.00.00) that routes the data outputs from each sub-element to the next sub-element in the processing chain.

The CSP architecture, graphically represented in Figure 3, is the result of multiple iterative design processes and reveals itself as the most suitable for ngVLA system requirements. The CSP follows an F-F-X architecture when operating in interferometric mode, and an F-B-F or F-F-B (where B stands for Beamforming) when operating in beamforming modes, depending on whether true-time delay or phase-shift beamforming is used, respectively.

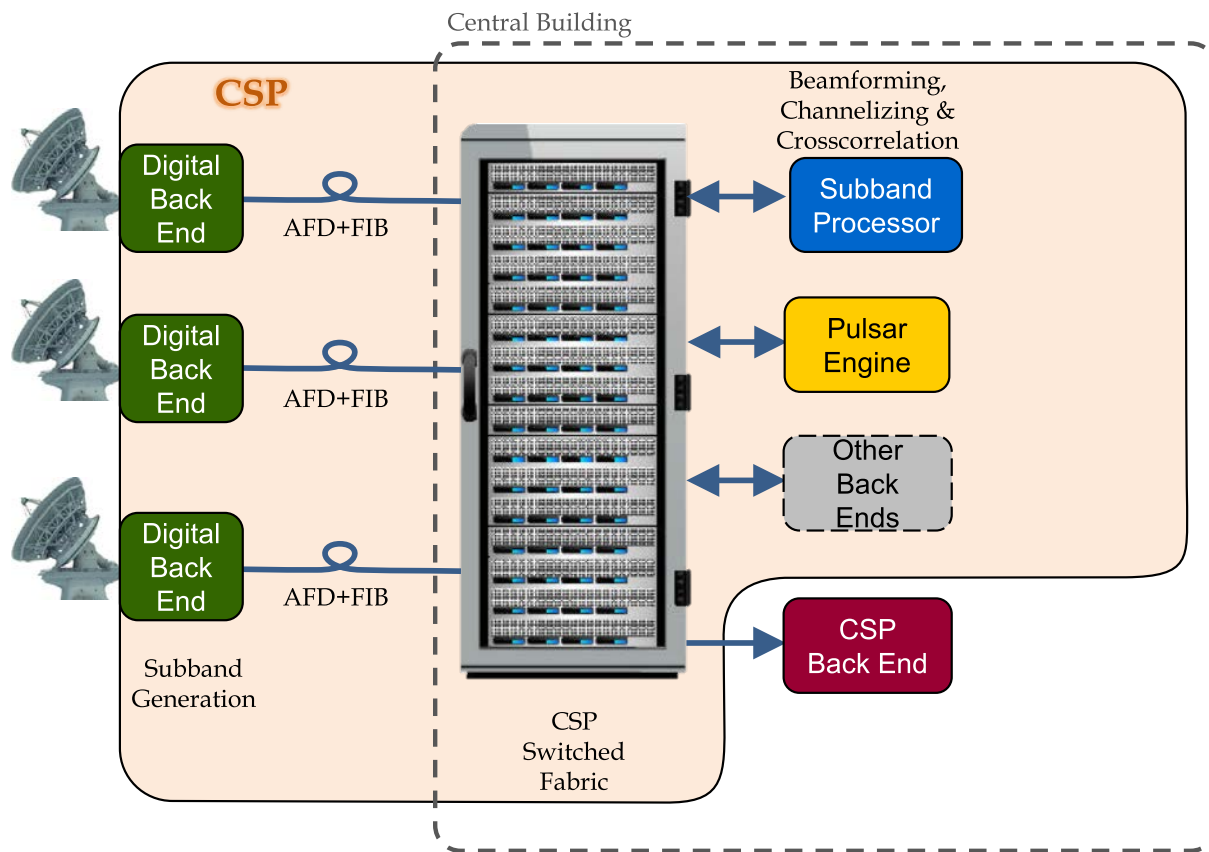


Figure 3: Central Signal Processor architecture.

Regardless of the operation mode, the first F-Engine that splits the digitized voltage into frequency sub-bands is implemented by the DBE. The DBE is located at the antenna sites, with the option of moving some of the units into the same building as the rest of the CSP for the closest sites located within the IRD range. The remaining mode-dependent stages are carried out by the SBP, consisting of a set of independent units each one processing a pair of sub-bands (or a single sub-band in high-res mode). The SBP is in the central processing building. The data from the various antennas' DBE are routed to the proper SBP unit

Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

by the CSF, also located in the central processor building. When required by an observation, the data from the SBP can be sent to the PSE via the CSF for additional processing.

The CSP output for the CSS subsystem can be generated by the SBP and the PSE. Since they both connect via the CSF, ideally the CSS subsystem will connect to both sub-elements through the CSF as well. The alternative is to provide a separate network through which the SBP and the PSE can transmit their data products to the CSS. On the other hand, a communications network different from the CSF will carry the monitor and control data between the CSP and the CSS. Although it is unlikely that such network will possess the capacity to sustain the CSP scientific data output throughput.

In addition to the DBE, the SBP, and the PSE, the CSF will also provide enough spigots to allow any additional custom back ends to subscribe to sub-band data from the DBE, finely channelized² or beamformed data from the SBP, correlated data from the SBP (a.k.a. visibilities), or dedispersed and/or time folded data from the PSE. If the CSS is finally connected to the CSF, the output of those custom back ends may be sent to it for archiving purposes.

Figure 4 represents the CSP system architecture model. Notably, the DBE is not included in this model, as it belongs to the architecture model of the Antenna Electronics subsystem (CI number 020.30.00.00.00).

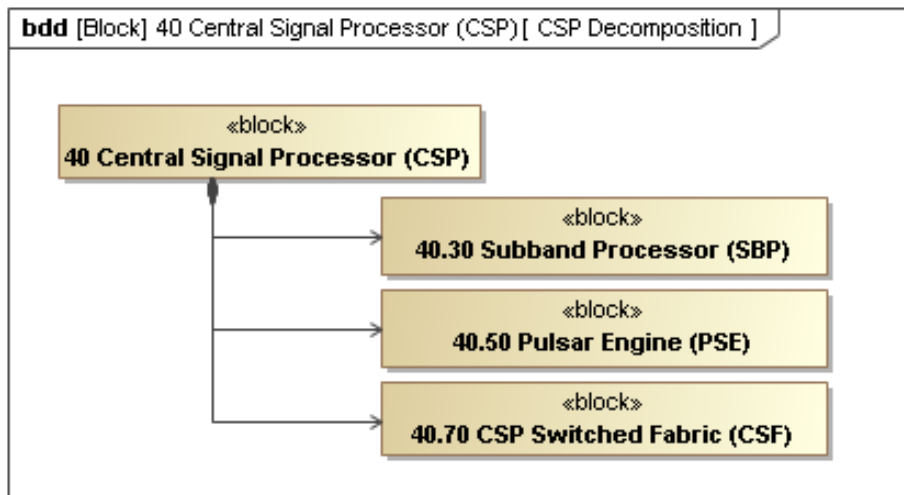


Figure 4: Central Signal Processor system architecture model.

3.3 Subsystem Functional Overview

The functional overview of the CSP is better understood from the respective functional overviews of its component parts.

The functional diagram of the DBE is shown in Figure 5 (next page). The diagram only represents the data flow of one receiver, so that multiple receivers are processed equally in parallel. After receiving the digitized data from the IRD modules, the DBE applies a calibration filter on the received signal in order to equalize the spectrum and further suppress the unwanted sideband from the down conversion process, effectively performing sideband separation digitally. Then, a frequency shifter coarsely tunes the digitized spectrum and removes any per-antenna LO-shift as needed. After that, the bandwidth is split into frequency sub-bands through a filter bank. Finally, the selected sub-band data streams undergo a requantization process and the resulting data packets are timestamped for its transmission to the SBP.

² The data flowing from the second F-Engine to the X-Engine, that is, phase-delay-corrected finely frequency channelized data from each antenna, is only available for SCREAM-based SBP units.



Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

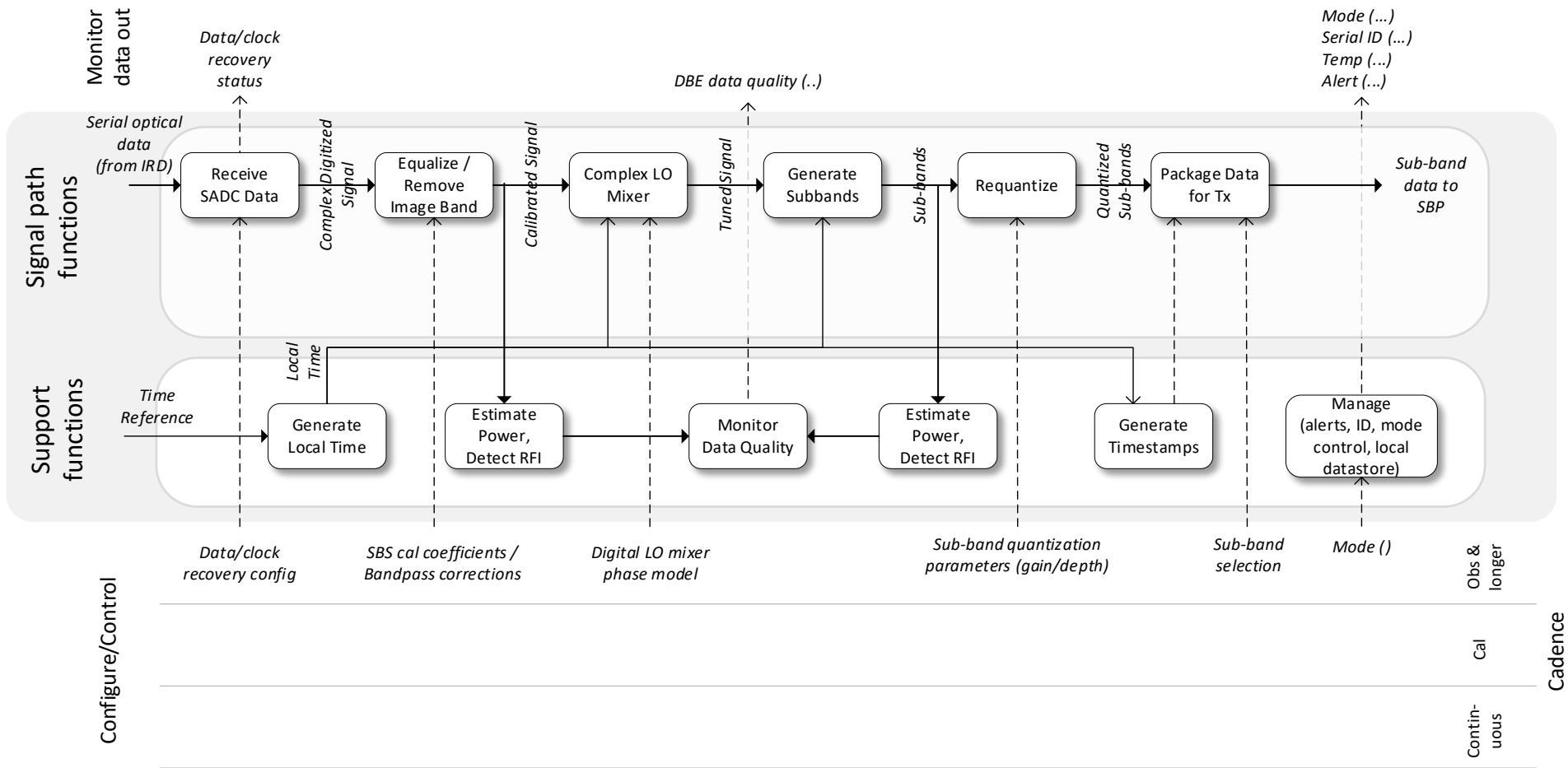


Figure 5: Functional overview of the Digital Back End.



Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

The sub-band processors receive data from all the antennas corresponding to one sub-band pair, or a single sub-band in high-res mode. Figure 6 (next page) depicts the functional diagram of the SBP in interferometric mode. The antenna data streams are first corrected for the bulk of the delay, which accounts for any variable network delay compensation, and then up-sampled to a common central reference time scale. This resampling process corrects the differences in sampling clocks at the various antenna sites. Next, a time-variable phase correction is applied, before finely channelizing the sub-band bandwidth into narrow frequency channels. Alternatively, spectral zooming involves a digital down conversion and decimation process prior to the frequency channelization. The resulting data streams are then requantized, packetized, and transmitted internally³ across the SBP computing nodes for cross-correlation. The correlator then performs a complex multiply-and-accumulate operation on a baseline pair basis according to the desired time resolution. Channel averaging may be carried out as well at the correlator. Finally, the uncalibrated visibilities are sent to the CBE for further processing and archiving.

In beamforming mode, the functional diagram of the SBP is slightly different, as represented in Figure 7. In this mode, which does not allow spectral zooming, the frequency channels from the antennas composing a subarray are linearly combined as opposed to cross-correlated. Different beamforming modes may be developed depending on the number of delay-phase trackers implemented and the number of linear combinations (beams) that are generated within an SBP.

The SBP also accepts hybrid interferometric–beamforming modes that generate a multiplicity of beams while also cross-correlating the data for one reference beam without involving a second SBP, in the same fashion as described by Figures 6 and 7 (next two pages).

The CSP also includes an ad hoc transient analysis back end, i.e., the Pulsar Engine (PSE), whose functional diagram is included in Figure 8. After receiving the data streams from the SBP via the CSF, data which normally correspond to the beamformed output, the PSE carries out a coherent dedispersion onto the data. This process may be preceded by a spectral rechannelization as needed. After dedispersion, Stokes parameters are generated through detection. Next, data can be folded according to a timing model and then integrated, or directly integrated in the absence of a timing model for transient search. The produced data is finally packetized and sent to the CBE for further processing.

³ A SCREAM-based SBP transmits the narrow frequency channels to the X-engine via the CSF. That’s why these data streams are accessible to a custom back end connected to the CSF.



Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

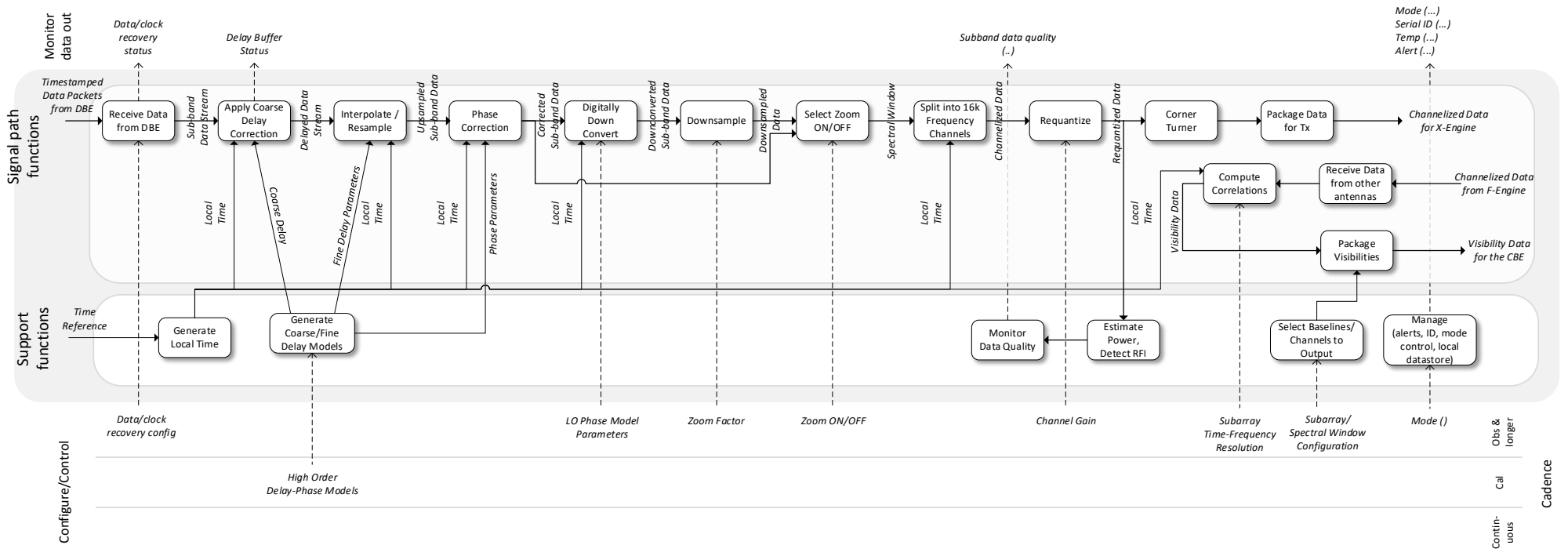


Figure 6: Functional overview of the Sub-band Processor operating in interferometric mode.



Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

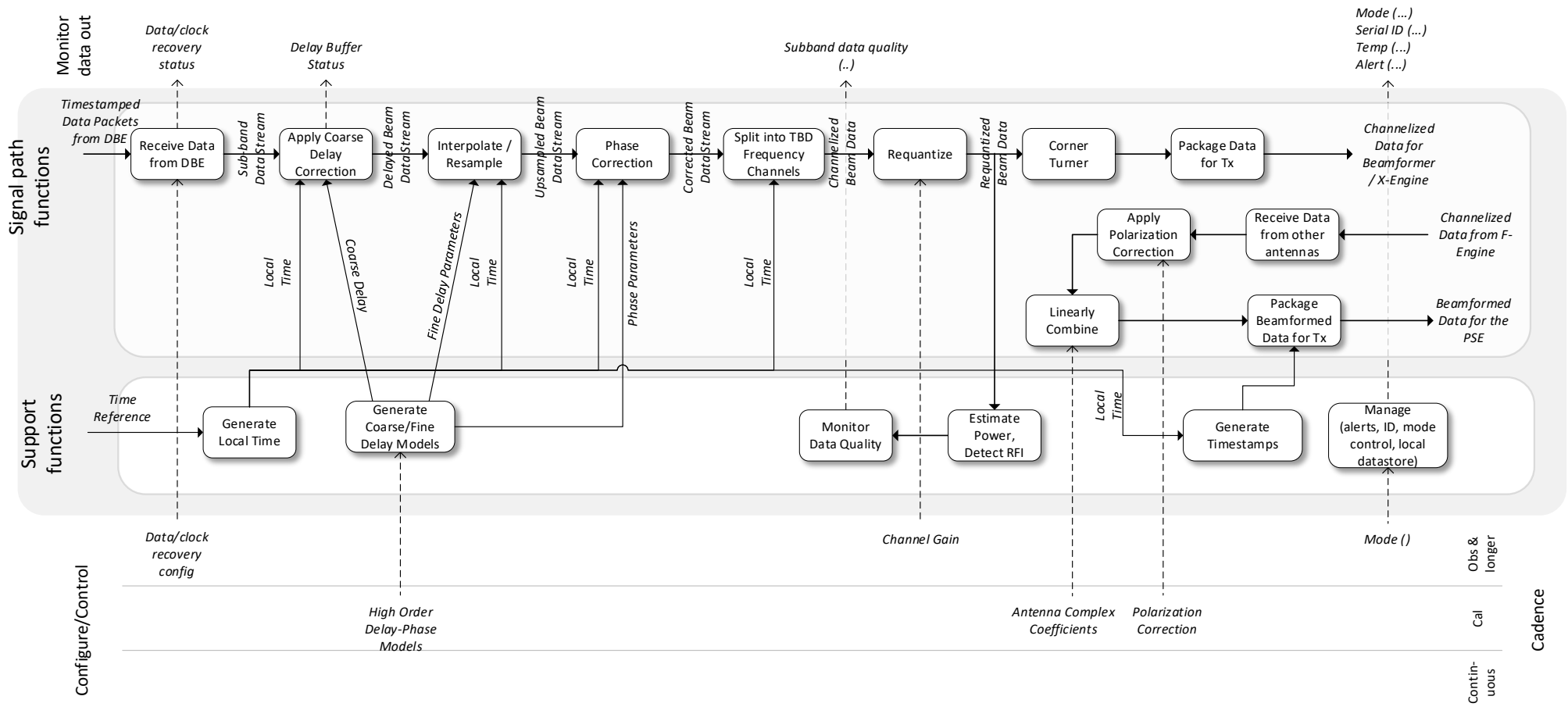


Figure 7: Functional overview of the Sub-Band Processor operating in beamforming mode.

Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

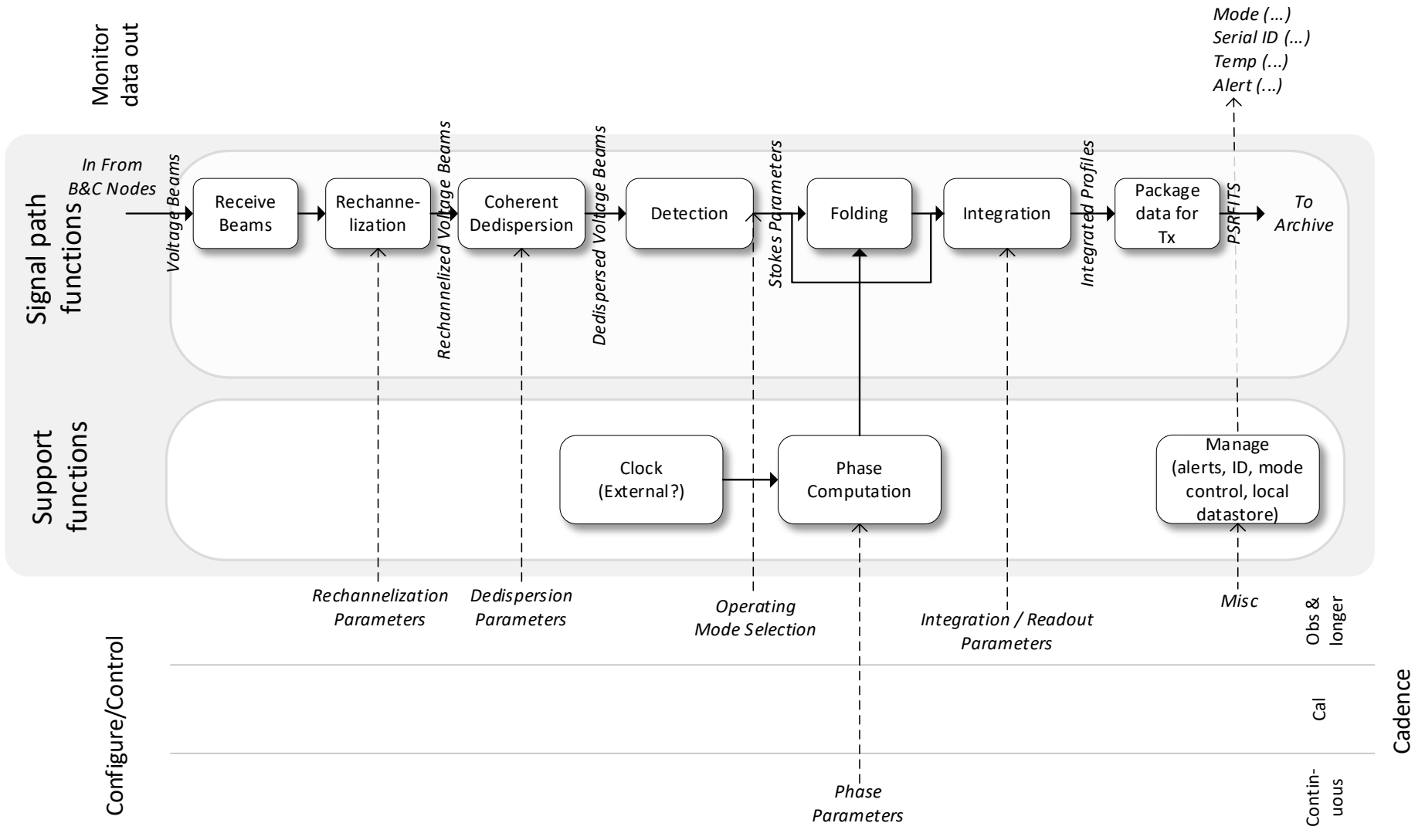


Figure 8: Functional overview of the Pulsar Engine.



Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

3.4 Design Driving Requirements

The following table provides a summary of the major design-driving subsystem requirements. Should there be a conflict between the requirements listed here and the descriptions in Section 7, the latter shall take precedence.

Parameter	Req. #	Value & design driver
Connected Antennas	CSP0006	The CSP shall support at least 263 dual-polarization antenna, full-bandwidth inputs, with a goal of fully scalable architecture. It drives the number of DBE Units and size of the SBP.
Per-Antenna Available Bandwidth	CSP0008	The CSP shall transmit and process at least 14 GHz of nonredundant bandwidth from every antenna polarization, or the full instantaneous bandwidth of the band in use, whichever is less, with a goal of a fully scalable architecture supporting at least 20 GHz.
Interferometric Bandwidth	CSP0021	The CSP shall support processing all the available bandwidth consistent with CSP0008 in interferometric mode.
Beamformer Bandwidth per Beam	CSP0030	The CSP shall be able to generate each beam with at least 8 GHz or the full instantaneous bandwidth of the band in use, whichever is less, with a goal of generating the full available bandwidth specified by CSP0008. Together, they drive the number of SBP Units.
Transient Bandwidth	CSP0038	The CSP shall support processing 8 GHz of bandwidth per beam, with a goal of all the receiver bandwidth in each band below 20 GHz.
Transient Number of Beams	CSP0039	The CSP shall support processing 10 full-bandwidth beams without dedispersion and folding, or 5 full-bandwidth beams with dedispersion and folding, with a goal of processing all the beams available at the beamformer output. Together, they drive the size of the PSE.
Correlation Loss	CSP0009	The correlation loss attributable to the CSP shall be less than 1%. It drives the computational precision of the CSP. CSP size and power highly depends on that precision. An SNR loss budget within the CSP is included within the CSP Performance Budgets [RD01].
Commensal Signal Processors	CSP0014	The CSP switched fabric shall be scalable and allow flexible multicast for future commensal processing of visibilities and voltage data streams. It conditions the CSP architecture and network topology.
Beamformer Aperture	CSP0028	The CSP shall support full beamforming capabilities for any subarray (including extended baselines) with an aperture equal or less than SYS1301 specification (700 km).
Beamformer Field of View	CSP0031	The CSP shall support generating beams pointed at any direction within the antenna primary beam. This includes beamforming the SBA as well. Together, they can drive the internal memory requirements. Network latency is not so important if accommodated via external memory.
Subarray Independence	CSP0019	The configuration of a subarray shall be completely independent of all other subarrays operating on different antenna subsets. Support of subarray independence has deep implications in the architecture, size and operation of the CSP.

Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

4 Requirements Management

4.1 Requirements Definitions

Consistent with the Requirements Management Plan [AD02], the following definitions of requirement “levels” are used in the ngVLA program. The requirements in this document are at the L2 subsystem level.

Req. Level	Definition
L0	User requirements expressed in terms applicable to their needs or use cases (Science Requirements or Stakeholder Requirements)
L1	Requirements of the System, expressed in technical functional or performance terms (System Level Requirements)
L2	Requirements that define a specification for an element of the system, presuming a system architecture (Subsystem Requirements)

4.2 Requirements Flow Down

Figure 9 shows the relationships between the CSP subsystem (L2) requirements and the System (L1) Requirements from which they are derived. System Requirements include Security, Safety, and Environmental Specifications that apply to the CSP. They also include EMC and RFI Mitigation requirements. In an intermediate level between System and CSP requirements (L1.1), Electronics, Calibration and Technical Budgets requirements have been derived from the System Requirements and are applicable to the CSP subsystem as well.

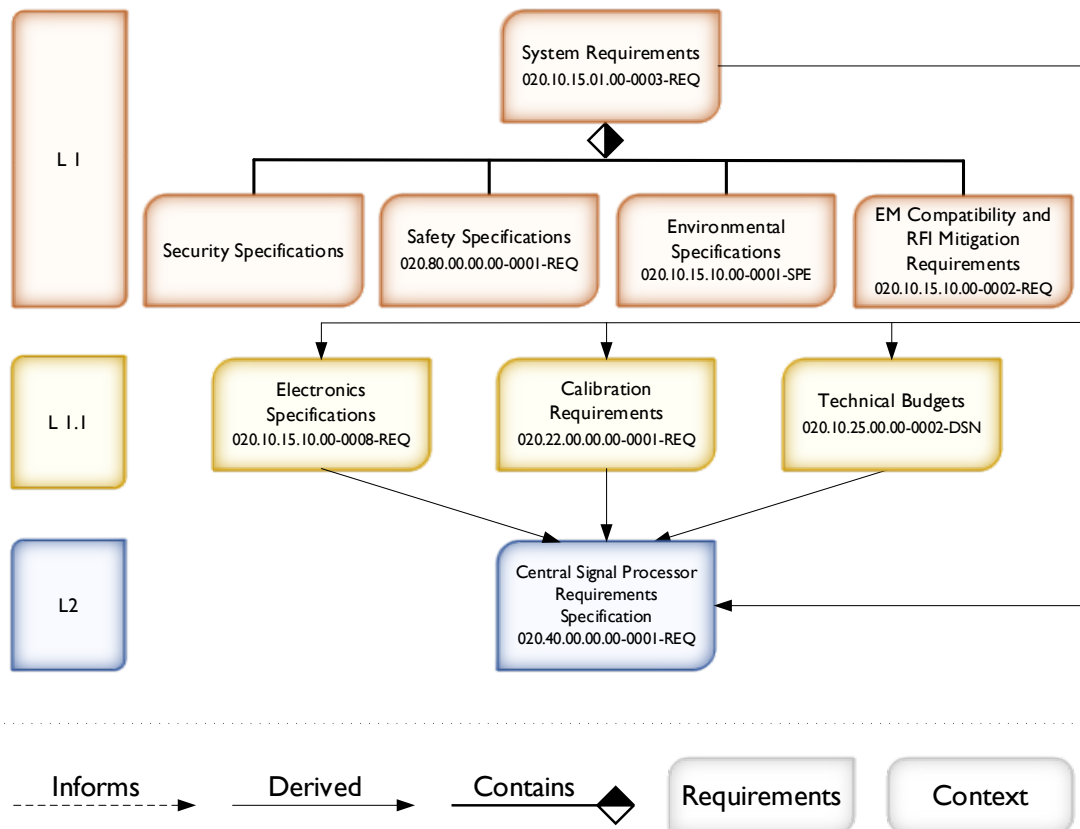


Figure 9: Requirements flow-down to the Central Signal Processor Subsystem Requirements.



Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

Individual subsystem specifications (Level 2) flow from the Level 1 requirements and may not always be directly attributable to a single system requirement. For example, phase drift specifications at the system level may be apportioned to multiple subsystems, or a subsystem spec may be in support of multiple higher-level requirements. Completeness of the Level 2 requirements is assessed at the requirements review of each subsystem.

While this is a top-down design process, the process is still iterative rather than a “waterfall” or linear process. The feasibility and cost of requirements implementation lead to trade-offs that feedback to higher-level requirements. The end goal is to build the most generally capable system that will support the Key Science Goals within the programmatic constraints of cost and schedule. Maintaining enumerated traceability between system requirements and subsystem requirements ensures that this trade-off process can be managed in a controlled way.

4.3 Verb Convention

This document uses “shall” to denote a requirement. The verbs “should” and “must” denote desired but not strictly required parameters. “Will” denotes a future happening. Desired but not required features are noted as “desirable” or “goals.”

5 Assumptions

The following assumptions are made in the definition of these subsystem requirements:

- Subsystem requirements apply to performance before any operational calibration corrections are applied unless explicitly stated otherwise.
- Hardware requirements apply to a properly functioning system under the precision operating environmental conditions unless explicitly stated otherwise.
- Hardware requirements assume that all system parts that would normally be in place during observations are working within their respective specifications (e.g., HVAC, RTP system) unless explicitly stated otherwise.
- Environmental requirements assume the antenna sites and ngVLA buildings are designed to host all corresponding CSP elements.
- Functional requirements assume the CSP architecture represented in Figure 3, where the sub-band bandwidth is fixed.
- Functional requirements assume filter-bank based frequency channelizers in the down-selection of the processed bandwidth.
- Functional requirements assume a quantization efficiency of the digitizer equal to or greater than 96%.
- Computation and application of the quantization correction is the responsibility of the Computing and Software System (CSS).
- Delay and phase model parameters are calculated by the Computing and Software System (CSS) subsystem and provided to the CSP. Thus, the CSS is responsible for compliance with System Requirements [AD03] in this regard, e.g., OTF mapping.
- Beamforming coefficients are computed by the CSS. Hence, the ultimate responsibility for generating nulling directions and controlling side lobes resides in the CSS.
- The support of per-baseline integration times does not include the CSP.
- The CSP is not responsible for recording the failure of its items in a FRACAS (Failure Reporting, Analysis, and Corrective Action System).



Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

6 Environmental Conditions

6.1 Normal Operating Conditions

All CSP equipment shall be installed in environmentally controlled facilities or racks. As such, the normal operating conditions are defined by the applicable ICD:

- [AD22] 020.10.40.05.00-0063 Antenna Bins, Modules, & Racks–DBE Interface Specification
- [AD25] 020.10.40.05.00-0098 ngVLA Site Buildings–Central Signal Processor Interface Specification

These ICD documents lead to the corresponding CSP requirements, as defined by CSP subsystem interface requirements in Section 7.2.3, and Section 7.2.6, respectively.

6.2 Transportation Conditions

Parameter	Req. #	Value	Traceability
Packaging for Transportation	CSP9001	All CSP LRUs shall be transported using ESD, thermal, shock and vibration protective packaging in accordance with the System Environmental [AD04] and Electronics Specifications [AD09].	ETR0503 ENV0381 ENV0382 ENV0531
Transportation Vibration Protection	CSP9007	All CSP LRUs packaged for transportation shall withstand persistent vibration with a power spectral density defined in Figure I of [AD04].	ENV0531
Mechanical Shocks	CSP9008	All CSP LRUs packaged for transportation shall survive mechanical shock levels from handling as defined in the MIL-STD-810H Method 516.8 Logistic Transit Drop Test, modified to use the drop heights specified in [AD04].	ENV0582

CSP9001 is a placeholder for future transportation conditions requirements.

CSP9007 is a copy of system environmental specification ENV0531. See [AD04] for additional details and rationale. DBE LRUs must meet CSP9007 when installed in the antenna.

CSP9008 is a copy of system environmental specification ENV0582. See [AD04] for additional details and rationale.

6.3 Storage Conditions

Parameter	Req. #	Value	Traceability
Packaging for Storage	CSP9002	All CSP LRUs shall be stored using ESD and thermal protective packaging in accordance with the System Environmental and Electronics Specifications.	ETR0503 ENV0372 ENV0373

6.4 Site Elevation

Parameter	Req. #	Value	Traceability
Altitude Range	CSP9003	All CSP elements shall be designed for operation and survival at altitudes ranging from sea level to 2500 m.	ENV0351



Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

6.5 Environmental Protection Requirements

6.5.1 Seismic

Parameter	Req. #	Value	Traceability
Seismic Protection	CSP9004	The CSP subsystem shall be designed to withstand a low-probability earthquake with up to 0.2g peak acceleration in either the vertical or horizontal axis.	ENV0521

CSP9005 is a copy of system environmental specification ENV0521. See [AD04] for additional details and rationale. The elements of the CSP shall not sustain residual damage under these conditions while in the installed and operational state.

6.5.2 Vibration

Parameter	Req. #	Value	Traceability
Vibration Protection	CSP9006	All CSP elements installed in the antenna shall withstand persistent vibration with a power spectral density defined in Figure 1 of [AD04].	ENV0531

CSP9005 is a copy of system environmental specification ENV0531. All DBE elements must meet CSP9005.

6.5.3 Mechanical Shock

No mechanical shock levels have been defined for the survival of the CSP LRUs when not packaged for transportation. See Section 6.2 for the shock levels defined for transportation conditions.

6.5.4 Lightning, Dust, Fauna, Solar Radiation, Rain/Water Infiltration, & Corrosion Protection

Protection against lightning, dust, fauna, solar radiation, rain/water infiltration and corrosion shall be provided by the environmentally controlled facilities or racks in which the CSP elements are installed, as defined by the applicable ICDs [AD22], [AD25]. No CSP element shall be installed outside these facilities or racks.



Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

7 Subsystem Requirements

7.1 Functional and Performance Requirements

7.1.1 Operating Mode Requirements

Parameter	Req. #	Value	Traceability
Interferometric Capabilities	CSP0001	The CSP shall support an operating mode that generates auto and cross-correlation estimates, i.e., visibilities.	SYS0001 SYS0002 SYS0007 SYS0008 SYS0102 SYS0103
Beamforming Capabilities	CSP0002	The CSP shall support an operating mode that generates dual polarization beamformed signals.	SYS0001 SYS0003 SYS0006 SYS0206
Transient Analysis Capabilities	CSP0003	The CSP shall support an operating mode that generates the polarization state (i.e., Stokes parameters) as a function of frequency and time or pulse phase.	SYS0001 SYS0004 SYS0005 SYS0742
Reconfiguration Time	CSP0004	The CSP shall be able to change the full configuration (including functional mode) of a subarray within 10 seconds or less from the time such a reconfiguration command is received.	SYS0009 SYS0908 SYS3005
Standby Mode	CSP0005	The CSP shall include a Standby functional mode where the status and health can be monitored with the goal of minimizing power consumption in this mode. This shall be the default mode.	SYS0010 SYS0011 SYS9990

The above Operating Mode Requirements provide a simple overview of the different functionality required from the CSP, grouped by the nature of the data product. Different Operating Modes demand different functional and performance requirements. Such requirements are specified in the following sections. The CSP design can develop as many functional modes as needed to fully cover the functional and performance parameter space.

System Interferometric, Total Power, and On-The-Fly Mapping Modes govern the interferometric capabilities of the CSP; System Phased Array and VLBI Modes define the beamforming capabilities of the CSP; and System's Pulsar Timing and Pulsar and Transient Search Mode are supported by the transient analysis capabilities of the CSP.

CSP0004 includes the reconfiguration of the DBE, and specifically the reconfiguration of the sub-bands selected for further processing, previously specified by CSP0047. It is not assumed that the network delay to receive the reconfiguration command is included in CSP0004.

CSP0005 defines the Standby Mode as the default mode. The default mode is the functional mode to which the CSP must default in the absence of a proper functional mode command.



Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

7.1.2 General Functional and Performance Requirements

Parameter	Req. #	Value	Traceability
Connected Antennas	CSP0006	The CSP shall support at least 263 dual-polarization antennas, full-bandwidth inputs, with a goal of fully scalable architecture.	SYS1021 SYS1001 SYS1309
Polarization	CSP0007	The CSP shall allow processing both polarizations in all its Operating Modes.	SYS1900 SYS0102 SYS0207 SYS0305 SYS6104
Per-Antenna Available Bandwidth	CSP0008	The CSP shall transmit and process at least 14 GHz of nonredundant bandwidth from every antenna polarization, or the full instantaneous bandwidth of the band in use, whichever is less, with a goal of a fully scalable architecture supporting at least 20 GHz.	SYS0903
Correlation Loss	CSP0009	The correlation loss attributable to the CSP shall be less than 1%.	SYS1033 SYS1034 SYS1035
Longest Baseline	CSP0010	The CSP shall support extended baselines (VLB) out to 8800 km.	SYS1301
Number of frequency channels	CSP0011	The CSP shall support at least 240,000 frequency channels (per polarization) in both interferometric and beamforming modes, with a goal of 2,000,000 channels.	SYS1402
Timing Accuracy	CSP0012	The timing error introduced by the CSP shall be consistent with the timing error budget of the system.	SYS2002 SYS2003
Polarization Dynamic Range	CSP0013	Any polarization transformation within the CSP shall support the polarization dynamic range established in SYS6104 (35 dB at < 8 GHz).	SYS1902 SYS6104
Commensal Signal Processors	CSP0014	The CSP switched fabric shall be scalable and allow flexible multicast for future commensal processing of visibilities and voltage data streams.	SYS0502 SYS5600 SYS5601 SYS5602 SYS5603
Self-Generated Spurious Signal Power Level	CSP0015	The CSP shall not generate spurious signals above -43 dB relative to the system noise level on cold sky over a 1 MHz bandwidth.	SYS2104

The number of antennas and the processed instantaneous bandwidth determine the computational requirements of the CSP. For long-term value, it is desired that the CSP architecture is inherently scalable to any number of antenna inputs or receiver bandwidth. This mitigates the risk of future hardware upgrades not providing enough value to justify the replacement of the old hardware. It also facilitates a gradual deployment of the CSP in several phases.

CSP0006 emanates from the current array configuration. This configuration concept defines a 263-antenna ngVLA, arranged as 214 antennas for the main array, 19 antennas for the SBA (Short Baseline Array), and 30 antennas for the LBA (Long Baseline Array). The preferred design will be scalable to any given number of antennas, as opposed to a constrained architecture.

The non-redundant bandwidth transmitted from every antenna (CSP0008) determines the maximum bandwidth that can be processed in each Operating Mode. This does not mean the CSP must process all the available bandwidth in all Operating Modes. Simultaneous subarray operation or specific Operating



Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

Modes may impose additional constraints in the amount of bandwidth processed, as specified in the following sections. However, processing 20 GHz of bandwidth in any Operating Mode might be desirable in the future [RD02], justifying the goal of a scalable design.

The CSP correlation loss in CSP0009 assumes a digitizer quantization efficiency of 96%, so that the total correlation loss does not exceed 5%. An SNR loss budget within the CSP is included within the CSP Performance Budgets [RD01]. This is in accordance with the current system technical budget for digital efficiency [AD10]. Digital correlation losses are generally introduced whenever the data are approximated by their finite precision representation, where the data could correspond to many different parameters, such as signals, delays, phases, (filter) coefficients, or correlation estimates. Although this requirement formally is only applicable in interferometric mode, it affects the common per-antenna processing chain of all operating modes and thus has been included along with general requirements.

CSP0009 applies to all frequencies within the system frequency span defined by SYS0803, SYS0804, and SYS0805, under the assumption that digitization efficiency is also satisfied. The CSP frequency channelization strategy shall guarantee that this requirement can be satisfied without gaps in frequency coverage. For example, sufficient spectral overlap across sub-bands shall be allocated so that the frequency channels at the sub-band edges that do not satisfy CSP0009 are discarded (the adjacent sub-bands satisfy CSP0009 for the corresponding RF band).

CSP0011 allows the CSP to operate in coarser frequency resolutions as a function of the overall bandwidth so that the resulting number of channels does not exceed the specified value. The highest spectral resolution is specified below depending on the Operating Mode.

Although data processing within the CSP is digital, subsample delay correction may introduce additional frequency-dependent uncertainty in the timing of signals. The error incurred must be consistent with System Technical Budgets [AD10]. For context, the maximum system error established by SYS2002 is 10 ns, with a goal of 1 ns. It is expected that any systematic timing error introduced by the CSP can be corrected in postprocessing.

Commensal Signal Processors are inherently supported by the assumed CSP architecture, but it must be enabled by supporting multicast capabilities.

7.1.3 Subarray Operation Requirements

Parameter	Req. #	Value	Traceability
Subarray Operation	CSP0016	The CSP shall support operation in subarray mode, where each subarray employs an arbitrary subset of antennas.	SYS0601 SYS0603
Number of Subarrays	CSP0017	The CSP shall support simultaneous operation of at least 10 subarrays.	SYS0601
Simultaneous Subarray Capabilities	CSP0018	The CSP shall support subarray operation with combinations and capabilities equal to or greater than the functionality described in [AD03].	SYS0604 SYS0605
Subarray Independence	CSP0019	The configuration of a subarray shall be completely independent of all other subarrays operating on different antenna subsets.	SYS0606 SYS0608
Subarray Reconfiguration	CSP0020	The CSP shall support adding and subtracting elements from a subarray without interrupting an observation.	SYS0602 SYS0607



Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

Parameter	Req. #	Value	Traceability
Secondary Subarray Capabilities	CSP0058	The CSP shall support “secondary” subarrays, i.e., subarrays operating on the same antenna subset and RF band as an existing subarray (the “primary” subarray). The configuration of the operating mode and phase-delay model of secondary subarrays shall be independent of primary subarrays.	SYS0606 SYS0608

The rationale behind CSP0058 is to enable observing one or multiple sources, within the primary beam of the antennas in the subarray, with different operating modes, e.g., interferometric and beamforming. An additional motivation is to increase the number of phase-delay tracking centers allowed in a single operating mode by trading bandwidth in as needed. Secondary subarrays may be used to pursue different scientific goals (despite operating on the same antenna subset and RF band), as well as to expand the capabilities of the CSP beyond the requirements defined herein, but generally by trading in some other CSP capability (e.g., bandwidth for multiple phase centers, as described above).

To understand CSP0019 and CSP0058, Subarray Independence and Secondary Subarray Capabilities, it is convenient to make a distinction between primary and secondary subarrays:

- Primary subarrays are those carrying out observations in independent (disjoint) subsets of antennas.
- Secondary subarrays are those carrying out commensal observations using a subset of antennas already in use by a primary subarray. Secondary subarrays must operate in the same frequency band as the primary subarray.

The configuration and operation of a secondary subarray cannot be fully independent from its associated primary array, or any other secondary subarray operating on the same antenna subset. However, requiring independent configuration and operation among primary subarrays should not be problematic at the CSP level.

From System Requirements [AD03], a subarray’s antenna configuration is such that the whole array is split into disjoint sets of antennas assigned to subarrays. A single subset of antennas can be assigned to multiple subarrays, with only one of them being the primary subarray. The antenna configuration, including the DBE, is determined by the primary subarray and constrains the capabilities of secondary subarrays, such as pointing direction and receiver feed. In addition, the frequency sub-bands that are available to secondary subarrays may also be limited by the maximum available bandwidth per antenna (see CSP0008 for minimum required capabilities).

The subarray configuration process becomes as follows: An arbitrary antenna configuration, from one antenna to the whole array, is selected for the first subarray created, always a primary subarray. For the second subarray, either the already existing subset of antennas is used, hence, becoming a secondary subarray, or a new subset is created using only the available antennas not used by the first subarray, becoming a second primary subarray. At any given time, a newly created subarray may use the same antenna subset as any of the existing subarrays or create a new arbitrary subset from the unused antennas.

CSP0020 is direct consequence from System Requirements [AD03]. In this regard, System Requirements clarify that “[...] the addition or subtraction of array elements from a subarray needn't be immediate, and can occur at a natural boundary point such as a scan boundary.”



Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

7.1.4 Interferometric Requirements

Parameter	Req. #	Value	Traceability
Interferometric Bandwidth	CSP0021	The CSP shall support processing all the available bandwidth consistent with CSP0008 in interferometric mode.	CSP0008
Interferometric Frequency Resolution	CSP0022	The highest frequency resolution in interferometric observations shall be at least 1 kHz, with a goal of 400 Hz.	SYS1401
Interferometric Variable Frequency Resolution	CSP0023	The CSP shall support independent frequency resolution settings per sub-band in interferometric observations.	SYS1403
Interferometric Time Resolution	CSP0024	The CSP shall support correlation integration times between 100 ms and 5 s, with a goal of starting at 1 ms intervals.	SYS0106 SYS2001
Interferometric Channel Flatness	CSP0025	The in-band frequency response of any CSP frequency channel (e.g., channel passband ripple) shall be consistent with CSP correlation loss requirements.	CSP0009 SYS1701 SYS1702 SYS1703
Interferometric Frequency Selectivity	CSP0026	The channel frequency response of the CSP in interferometric mode shall be, relative to the channel center, -3.01 ± 0.01 dB at the channel edge, -60 dB or better at the center of the adjacent channel, and -80 dB or better beyond the adjacent channel edge, with a goal of reaching -80 dB at the center of the adjacent channel and beyond.	SYS6105 SYS6106
Interferometric Polarization Products	CSP0027	The CSP shall allow generating any combination of the four parallel-pol and cross-pol correlations within a subarray.	SYS0102 SYS0105

It is assumed that frequency resolution in interferometric mode will be configurable. Otherwise, at least 14 million frequency channels must be supported to be consistent with the required maximum bandwidth.

The call for independent sub-band frequency resolution originates from the need for accommodating spectral line and continuum observations in a single setting, as described in System Requirements [AD03].

Similarly, integration time at the X-Engine must be configurable within the values in CSP0024. The goal of starting at 1ms intervals in CSP0024 refers to the minimum time resolution, not the quantization step of the configurable time resolutions. Using a logarithmic set of values as the configurable time resolutions may be acceptable, e.g., [100ms, 200ms, 400ms, ...]. OTF modes have been included within the supported range, as the scan mode makes no qualitative difference in the CSP operation. The CBE input data rate may limit the total bandwidth that can be observed at the shortest integration times. Any configuration demanding per-baseline integration times will be satisfied by the CSS.

The frequency response of the CSP within the band of a frequency channel produces a correlation or SNR loss with respect to an ideal rectangular function. The effect of slope, ripple, etc., can be computed according to formulas described [RD03, RD04]. For example, for a correlation loss of 0.05%, the maximum sinusoidal peak-to-peak ripple in an otherwise perfectly rectangular channel should be less than 0.39 dB.



Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

The frequency selectivity specified in interferometric mode satisfies the System emissive dynamic range requirement SYS6106. It also satisfies the absorptive dynamic range SYS6105 assuming certain decreasing trend of the sidelobe level. Quantization of the window coefficients must also be considered as it could limit the sidelobe decay.

7.1.5 Beamforming Requirements

Parameter	Req. #	Value	Traceability
Beamformer Aperture	CSP0028	The CSP shall support full beamforming capabilities for any subarray (including extended baselines) with an aperture equal or less than SYS1301 specification (700 km).	SYS0201 SYS1301
Number of Beams	CSP0029	The CSP shall support producing a minimum of 10 beams, with a goal of 50 beams, distributed over the active subarrays.	SYS0203 SYS0301 SYS0401 SYS0501
Beamformer Bandwidth per Beam	CSP0030	The CSP shall be able to generate each beam with at least 8 GHz or the full instantaneous bandwidth of the band in use, whichever is less, with a goal of generating the full available bandwidth specified by CSP0008.	SYS0302 SYS0402 SYS0505
Beamformer Field of View	CSP0031	The CSP shall support generating beams pointed at any direction within the antenna primary beam. This includes beamforming the SBA as well.	SYS0205
Beamforming SNR Efficiency	CSP0032	The CSP shall generate a beamformer output with an SNR at least 95% of what an ideal beamformer would produce for the same inputs.	SYS0208
Beamformer Polarization Correction	CSP0033	The CSP shall support per-antenna polarization calibration in beamforming mode.	SYS0207 CSP0032
Concurrent Interferometric Mode	CSP0034	The CSP shall generate cross-correlation products for one of the phase centers while operating in beamforming mode. The bandwidth processed, as well as the time and frequency resolutions of these cross-correlation products might satisfy lower specifications than the interferometric requirements in Section 7.1.4. (TBD)	SYS0202 SYS0209 SYS1061 SYS4310 SYS4311
VLBI Support	CSP0035	The CSP shall be able to select the bandwidth and format the output of the beamformer in compliance with bandwidth and quantization specifications in support of VLBI Observing Mode.	SYS0503 SYS0504 SYS0745 SYS0746

CSP0028 is specified for the minimum aperture of the Main Array as defined in SYS1301. It is understood that the intent is to support beamforming capabilities for the true final configuration of the Main Array, which likely will increase the aperture.

When provided with the proper beamforming and polarization calibration coefficients, the beamformed radiation pattern can meet polarization dynamic range requirements, include nulling directions, and control its side-lobe level, as per System Requirements [AD03]. Therefore, the responsibility of such capabilities lies in the subsystem generating those coefficients.



Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

The above requirements define functional and performance capabilities of the beamforming operating mode.

As per System Requirements [AD03]: “The need for phased array capability over the full main array is due to the expected sub-array allocations. [...] The use of the main array aperture size in this definition is not intended to preclude using the extended baselines [...] so long as the phased sub-array does not exceed 700 km in extent.”

The number of beams is for the whole array. Hence, it must be distributed over subarrays in this operating mode.

CSP0029 accounts for the most demanding use case, currently specified by SYS0203 (Phased Array Operating Mode), SYS0301 (Transient Timing Operating Mode), SYS0401 (Transient Search Operating Mode), and SYS0501 (VLBI Operating Mode) demand less or equal capabilities.

Concurrent visibilities required by CSP0034 are required for calibration purposes. It is expected that the interferometric phase center is located on a calibrator within the primary beam of the antenna.

Compatibility with a standard VLBI format, e.g., VDIF, is expected.

7.1.6 Transient Analysis Requirements

Parameter	Req. #	Value	Traceability
Transient Stokes Parameters	CSP0036	The CSP shall produce all Stokes parameters when operating in transient analysis modes.	SYS0305 SYS0405
Dedispersion and Folding Capabilities	CSP0037	The CSP shall support dedispersion and folding for generation of pulse profiles.	SYS0741 SYS0407
Transient Analysis Bandwidth	CSP0038	The CSP shall support processing 8 GHz of bandwidth per beam, with a goal of all the receiver bandwidth in each band below 20 GHz.	SYS0302
Transient Analysis Number of Beams	CSP0039	The CSP shall support processing 10 full-bandwidth beams without dedispersion and folding, or 5 full-bandwidth beams with dedispersion and folding, with a goal of processing all the beams available at the beamformer output.	SYS0301 SYS0401
Transient Analysis Time Resolution	CSP0040	The CSP shall allow adjusting the time resolution, with the highest resolution equal or better than 488 ns.	SYS0304 SYS0306 SYS0404
Transient Analysis Frequency Resolution	CSP0041	The CSP shall support a frequency resolution of at least 1 MHz, with a goal of 50 kHz.	SYS0303 SYS0403
Transient Analysis SNR Efficiency	CSP0042	The CSP shall generate a transient analysis output with an SNR at least 95% of what an ideal processor would produce for the same inputs.	SYS0309 SYS0406

The above requirements define the performance and functional requirements of the Transient Analysis Operating Mode of the CSP. This mode is performed at the PSE, which will usually operate on the beamformed outputs of the SBP. The above requirements apply to both pulsar timing and transient search functionalities.



Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

The minimum time resolution is determined by the need of generating 2048 “bins” within a 1-ms pulse profile. This is more than what is needed when searching for transients. The time resolution will need to increase to throttle the output data rate. For context, a 14-ms time resolution would be consistent with generating 2048 bins in a 30-s pulse.

The time and frequency resolutions are dependent on each other. Finely frequency-channelized data will inherently have a poor time-resolution. The product of both resolutions will always be at least a few times greater than one, i.e., no oversampling.

The transient SNR efficiency is separate from other efficiencies specified, particularly, beamforming SNR efficiency (CSP0032).

It has not been defined yet whether the CSP or the CSS will be responsible for formatting the output in PSRFITS format, as required by SYS0741 and SYS0742.

7.1.7 Sideband Separation Requirements

Parameter	Req. #	Value	Traceability
Sideband Separation	CSP0043	The CSP shall apply sideband separation and equalization filters to the receiver digitized signal.	SYS1704
Sideband Separation Level	CSP0057	When provided with ideal (error-free) sideband separation calibration coefficient, the CSP shall achieve an unwanted sideband rejection greater than TBD (>30 dB, goal of >40 dB) within the usable bandwidth.	SYS1704

The sideband separation specification in CSP0043 will need to support the spectral dynamic range requirement and imaging fidelity requirement. System Requirements [AD03] call for at least 30 dB rejection, with a goal of 40 dB after the application of digital sideband separation techniques. It is currently assumed that the DBE will apply these techniques. It is desirable that the filter coefficients be stored by the DBE instead of transmitted through the interface with the Monitor and Control subsystem, but this possibility is still to be determined.

CSP0057 is a placeholder for a future requirement limiting the decrease in image rejection due to precision loss in the CSP. An appropriate system budget is needed before this requirement can be defined. The usable bandwidth is the portion of the input bandwidth that may produce a frequency channel at the CSP output. For example, the edges of a receiver band and the LO frequency should not be part of the usable bandwidth of that specific receiver. In the future, System Requirements may develop different goals depending on the observing mode, e.g., beamforming, interferometric, or total power. Even so, the CSP will most likely have to meet the highest standard as long as the digital sideband separation is performed by the DBE, which is observing-mode independent.

7.1.8 Sub-Band Generation Requirements

Parameter	Req. #	Value	Traceability
Sub-band Generation	CSP0044	The CSP shall split the receiver’s output signal into frequency sub-bands.	SYS0905
Sub-Band Selection	CSP0045	It shall be possible to select any arbitrary subset of sub-bands within the frequency band in use that does not exceed the bandwidth limit specified by CSP0008.	SYS0905
Sub-band Bandwidth	CSP0046	The sub-band bandwidth shall be 250 MHz or smaller.	SYS0907



Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

Parameter	Req. #	Value	Traceability
Sub-band Selection Reconfiguration Time	CSP0047	Superseded by CSP0004,	
LO Offset Support	CSP0048	The CSP sub-band generation process shall compensate for LO offsets at the antenna level as necessary.	SYS2105

For some frequency bands, the receiver output bandwidth may exceed the CSP computational capabilities or the network infrastructure’s available throughput. As per System Requirements [AD03], the CSP is the subsystem responsible to down-select the portion of bandwidth that shall be transmitted and processed. This is achieved by splitting the digitized bandwidth into frequency sub-bands at the antenna site.

The CSP architecture represented in Figure 3 calls for a fixed sub-band bandwidth, which, along with the use of filter-bank based frequency channelizers, makes the sub-band bandwidth directly constrained by SYS0907, “Sub-Band Step Size.”

SYS0908, “Band Switching Time,” dictates how fast the bandwidth selection configuration must change, as this cannot be preserved across different frequency bands.

The implementation of LO offsets at the antenna level might require the CSP to compensate for it prior to sub-band generation, which must be considered in the CSP design.

7.1.9 RFI Mitigation Requirements

Parameter	Req. #	Value	Traceability
RFI Mitigation	CSP0049	It is a goal that the CSP implement RFI mitigation algorithms that can be deactivated.	SYS2604 SYS4100 SYS4101 SYS4102

The need for RFI mitigation algorithms within the CSP has to be determined by assessing their effectiveness and a thorough characterization of the ngVLA radio environment.

7.1.10 Delay and Phase Tracking Requirements

Parameter	Req. #	Value	Traceability
Geometric Delay	CSP0050	The CSP shall compensate for geometric and atmospheric delays in accordance with CSP0010 (baselines up to 8800 km long) and for any observing elevation angle.	CSP0010 SYS0108 SYS0602 SYS1102
Delay and Phase Tracking Update Rate	CSP0051	The system shall be able to update the delay and phase corrections at a rate of at least 10 Hz, with a goal of 20 Hz. (TBC)	SYS5700 SYS5701 SYS5702 SYS0204 SYS0205
Sampler Clock Offset Support	CSP0052	It is a goal that the CSP delay and phase tracking process supports compensating for a digitizer clock offset.	SYS2105
Delay and Phase Tracking SNR Loss	CSP0053	The SNR loss incurred by the CSP with respect to an ideal delay and phase tracker with the same inputs shall not exceed its maximum allowance in System Technical Budgets [AD10]. (1% is allowed for the System)	SYS1502 [AD10]



Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

The above requirements apply to both interferometric and beamforming modes. The update rate is determined by interferometric mode requirements.

For context, the maximum geometric delay in 10,000-km baselines is 3.3 ms, which is small compared to the expected network latency (more details in the specific interface requirements below). However, the geometric delay compensation requirement applies to the main phase center position. Multiple phase centers will require differential delay corrections and are fully supported (i.e., anywhere within the same antenna lobe) only for the beamforming-specific aperture limit; see CSP0028.

Moreover, it is assumed that the phase and delay correction model parameters are computed by the CSS. Therefore, requirements such as SYS0602 (array phase center preservation) or the location of the array phase center have no impact on CSP requirements.

The delay and phase tracking update rate does not refer to the rate at which the CSP receives new data (delay and phase models) from the CSS, which can be much slower, but the rate at which the corrections derived from the model are updated. These requirements have been derived in the System Requirements document [AD03] and support OTF mapping at super-sidereal tracking rates. The current design concept applies first order delay/phase models at the sub-band sampling frequency, which is orders of magnitude faster than the goal.

As per System Requirements, dynamic Doppler tracking is not required.

7.1.11 Dedispersion Requirements

Parameter	Req. #	Value	Traceability
Dispersion Measure Range	CSP0054	The CSP shall be able to compensate for dispersion measures up to 3000 pc/cm ³ .	SYS0308

7.1.12 Folding Requirements

Parameter	Req. #	Value	Traceability
Pulse Profile Bins	CSP0055	The CSP shall generate a minimum of 2048 pulse profile bins.	SYS0304
Pulse Period	CSP0056	The CSP shall be capable of folding for pulse periods spanning from 1 msec to 30 sec.	SYS0306

7.2 Interface Requirements

In this section, requirements are derived from the applicable ICDs as listed in Section 2.2. As stated in the SEMP [AD01], ICDs define the interface, but do not contain any requirements. All interface requirements that drive the design and verification of the subsystem shall be listed in this section.

Two sets of ICDs are included in the following: DBE ICDs and CSP ICDs. As the DBE is architecturally a separate element from the CSP, it uses its own set of ICDs.

Currently, most of the interface requirements are simple placeholders that will be fully developed during the PDR phase of the project.

7.2.1 020.10.40.05.00-0002 IRD–DBE Interface Requirements

The Integrated Receivers and Digitizers (IRD, CI number 020.30.15.00.00) provide the CSP with digital data. This interface has no mechanical requirements as the connection between the IRD and DBE subsystems is through the Antenna Fiber Distribution subsystem. It covers the data format, data rate, and number of data streams.



Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

Parameter	Req. #	Value	Traceability
Deterministic Input Data Buffer Latency	CSP1001	The DBE shall support returning to a known state of the input data buffer.	SYS2002 SYS2003 CSP0012
IRD Data BER	CSP1002	The BER of data coming from the IRD shall comply with specifications in [AD20].	[AD20]
IRD Data Integrity	CSP1003	No input samples shall be lost, e.g., a buffer overflow, from the IRD data stream.	SYS2002 SYS2003 CSP0012
IRD Data Clock Recovery	CSP1004	The DBE shall recover data clock from the IRD data stream.	0002_001
IRD Data Modulation	CSP1005	The DBE interface with IRD shall use PAM4 modulation at 56 Gb/s of data.	0002_007 0002_008 0002_009
IRD Data FEC Encoding	CSP1006	The DBE interface with IRD shall use industry standard 64b/66b FEC encoding, e.g., IEEE Std 802.3. (TBC)	[AD20]
IRD Data Deserialization	CSP1007	The DBE shall deserialize the input serial data stream as a 7 GS/s 8-bit data stream.	0002_001 0002_010
IRD Data Format	CSP1008	The DBE interface with IRD shall use the data format specified in [AD20].	0002_002

Deterministic latency is required because the timestamping process takes place within the DBE. The same reasoning applies to data integrity.

7.2.2 020.10.40.05.00-0006 Power Supply–DBE Interface Requirements

The DBE connects to the DC Power Supply sub-element (PSU, CI number 020.30.50.00.00), from which it receives power. This interface specifies the electrical signal and mechanical connector used in that interface.

Parameter	Req. #	Value	Traceability
DBE Power Interface	CSP1009	The DBE power interface shall comply with specifications defined in [AD21].	[AD21]



Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

7.2.3 020.10.40.05.00-0040 Antenna Bins, Modules, and Racks–DBE Interface Requirements

The antenna Bins, Modules, and Racks subsystem (BMR, CI number 020.30.55.00.00) hosts the DBE located at the antenna and provides it with an environmentally controlled space, structural support and RFI shielding. This interface defines the DBE dimensions, thermal load, EMI emissions, and fixing.

Parameter	Req. #	Value	Traceability
DBE Shielding	CSPI010	Superseded by CSPI014.	
DBE Safety Monitoring	CSPI011	Parameters that affect the health/safety of the DBE (e.g., temperature) shall be monitored by both the DBE and the BMR subsystems.	[AD22] SYS2502
DBE Dimensions	CSPI012	The DBE dimensions shall be compliant with specifications in [AD22].	[AD22]
DBE Thermal Load	CSPI013	The DBE thermal load shall be compliant with specifications in [AD22].	[AD22]
DBE RFI Emissions	CSPI014	The level of RFI emissions of the DBE equipment at each antenna shall not exceed the values in Table I.	ETR0601 EMC0310
DBE Fastening	CSPI015	The DBE shall use the fastening device defined in [AD22].	[AD22]
DBE Normal Operation Temperature	CSPI048	The DBE shall satisfy subsystem requirements for an ambient temperature within the range $0\text{ C} \leq T \leq 30\text{ C}$ (TBC).	[AD22] ETR0903
DBE Normal Operation Relative Humidity	CSPI049	The DBE shall satisfy subsystem requirements for an ambient relative humidity (non-condensing) within the range $30\% \leq RH \leq 70\%$ (TBC).	[AD22] ETR0903

Table I is derived from [AD05] by assuming at least 10 m between the DBE and the receiving elements, and an overall shielding from the RF room and the ARCS (the DBE housing) of at least 130 dB. Additional shielding may be obtained from the antenna pedestal wall. In addition to both EIRP limits in Table I, the DBE must also comply with pertinent regulations.

Frequency (GHz)		1	3	6	10	30	45	90
Spectral Line	Bandwidth, 0.1 km/s, (Hz)	333	1000	2000	3333	10000	15000	30000
	EIRP (dBm)	1	15	24	30	46	52	63
Continuum	Bandwidth, 0.1%, (MHz)	1	3	6	10	30	45	90
	EIRP (dBm)	19	32	41	48	63	69	80

Table I: Maximum EIRP from the DBE as a function of frequency, within the indicated bandwidth, so that the system sensitivity is not significantly degraded [AD05].



Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

7.2.4 020.10.40.05.00-0076 DBE–MCL System Interface Requirements

The Monitoring & Control sub-element (MCL, CI number 020.50.25.00.00) receives the health and status parameters of the DBE and provides it with configuration parameters as well as operational commands. This interface defines such parameters and commands, the communications protocols, and the physical interfaces.

Parameter	Req. #	Value	Traceability
DBE M&C Physical Interface	CSP1016	The DBE physical interface with MCL shall follow the specifications in [AD23].	[AD23]
DBE Monitor Data Rate	CSP1017	The DBE interface with MCL shall provide enough throughput in support of requirements defined in Section 7.4, Reliability, Availability, and Maintainability Requirements.	[AD23]
DBE Configuration Data Rate	CSP1018	The DBE interface with MCL interface shall provide enough throughput to effectively command and communicate configuration and applicable calibration parameters to the DBE, as specified in [AD23].	[AD23]
DBE Monitor Parameters	CSP1019	The DBE shall monitor and send via the M&C interface the set of parameters defined in [AD23].	[AD23]
DBE Configuration Protocol	CSP1020	The DBE shall support the configuration protocol and command set defined in [AD23].	[AD23]

7.2.5 020.10.40.05.00-0041 Antenna Fiber Distribution Interface Requirements

The DBE physically connects to the Antenna Fiber Optic subsystem (AFD, CI number 020.30.70.00.00) to receive digitized data from the IRD, and to output data towards the CSP facility. This interface defines the physical connection between DBE and AFD.

Parameter	Req. #	Value	Traceability
DBE Fiber Interface	CSP1021	The DBE interface with AFD shall follow the specifications in [AD24].	[AD24]
DBE Input Data Rate	CSP1022	The DBE interface with AFD shall support a data rate into the DBE in compliance with the DBE interface with the IRD.	[AD20] [AD24]
DBE Output Data Rate	CSP1023	The DBE interface with AFD shall support a data rate out from the DBE as defined in [AD24].	CSP0008 [AD24]

7.2.6 020.10.40.05.00-0095 ngVLA Site Buildings Interface Requirements

The ngVLA Site Buildings subsystem (NSB, CI number 020.61.10.00.00) hosts all CSP elements, except for those at the antenna, in a central facility that provides an environmentally controlled space, power, and RFI shielding. This interface defines the CSP dimensions, thermal load, EMI emissions, and fixing.

Parameter	Req. #	Value	Traceability
CSP Shielding	CSP1024	Superseded by CSP1028.	
CSP Safety Monitoring	CSP1025	Parameters that affect the health/safety of the CSP (e.g., temperature) shall be monitored by both the CSP and the NSB subsystems.	[AD25] SYS2502



Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

Parameter	Req. #	Value	Traceability
CSP Dimensions	CSP1026	The CSP dimensions shall be compliant with specifications in [AD25].	[AD25]
CSP Thermal Load	CSP1027	The CSP thermal load shall be compliant with specifications in [AD25].	[AD25]
CSP RFI Emissions	CSP1028	The CSP RFI emissions shall be compliant with specifications in [AD25].	[AD25] ETR0601 EMC0310
CSP Fastening	CSP1029	The CSP shall use the fastening device defined in [AD25].	[AD25]
Backup Power Operation	CSP1030	The NSB shall still be compliant with specifications in [AD25] in the event of an interruption of the main power system and while the CSP operates on a backup power system, e.g., environmental specifications.	[AD25]
CSP Immunity	CSP1045	The CSP shall comply with [AD25] immunity specifications.	[AD25]
CSP Normal Operation Temperature	CSP1046	The CSP shall satisfy subsystem requirements for an ambient temperature within the range $0\text{ C} \leq T \leq 30\text{ C}$ (TBC).	[AD25] ETR0903
CSP Normal Operation Relative Humidity	CSP1047	The CSP shall satisfy subsystem requirements for an ambient relative humidity (non-condensing) within the range $30\% \leq RH \leq 70\%$ (TBC).	[AD25] ETR0903
CSP Maximum Power Consumption	CSP1050	The overall power consumption of the CSP shall not exceed 2MW (TBC).	[AD25]

These ranges are generally supported by commercial electronic components. Subsystem requirements are defined in Section 7.

CSP1028 is a placeholder for a future requirement. The current assumption is that the CSP equipment complies with applicable commercial regulations, while the RFI shielding provided by NSB guarantees no significant degradation of the system sensitivity. This requirement will be determined from the ICD specification.

CSP1050 includes all equipment comprising the CSP. For example, it would include the coolant distribution units of a liquid cooling system used by the CSP, but not the HVAC equipment used for room temperature control.

7.2.7 020.10.40.05.00-0105 CSP–MCL System Interface Requirements

This interface aims to support the M&C data interface between the CSP at the central facility and the M&C subsystem (MCL, CI number 020.50.25.00.00). It provides defines the extent and cadence of monitor data, as well as configuration parameters and operational commands. It also specifies the communication protocols and the physical and mechanical interface between the CSP and MCL.

Parameter	Req. #	Value	Traceability
CSP M&C Physical Interface	CSP1031	The CSP physical interface with MCL shall follow the specifications in [AD26].	[AD26]



Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

Parameter	Req. #	Value	Traceability
CSP Configuration Data Rate	CSP1032	The CSP interface with MCL shall provide enough throughput to effectively command and communicate configuration and applicable calibration parameters to the CSP, as specified in [AD26].	[AD26]
CSP Monitor Parameters	CSP1033	The CSP shall monitor and send via the M&C interface the set of parameters defined in [AD26].	[AD26]
CSP Configuration Protocol	CSP1034	The CSP shall support the configuration protocol and command set defined in [AD26].	[AD26]

7.2.8 020.10.40.05.00-0114 CSP–Online Subsystem Interface Requirements

This interface supports the transmission of data and metadata generated by the CSP to the Computing and Software System (CSS, CI number 020.50.00.00.00), particularly the Online Sub-Element (ONL, CI number 020.50.10.00.00) [AD27]. The CSS is responsible for further processing the data as needed for calibration and archiving. This interface describes both the physical and logical specifications.

Parameter	Req. #	Value	Traceability
CSP Data Physical Interface	CSP1035	The CSP physical interface with ONL shall follow the specifications in [AD27].	[AD27]
CSP Output Data Rate	CSP1036	The CSP average and maximum output data rate shall not exceed the limits in [AD27].	CON104 CON105 [AD27]
CSP Output Data Format	CSP1037	The CSP data output shall use the communications protocol and data format specified in [AD27].	[AD27]

7.2.9 020.10.40.05.00-0119 CSP–Central Fiber Infrastructure Interface Requirements

The elements of the CSP at a central facility receive data from the antennas via the Central Fiber Optic Distribution subsystem (FIB, CI number 020.55.20.00.00). This interface is expected to use industry standards allowing high data rate (>100 Gb/s per link), long distance (~100 km) communications. The CSP must account for common operational capabilities of such systems. This interface aims at defining the physical specifications, but the logical specification belongs to a separate interface between the DBE and the SBP. Note that this interface must also cover the physical specification between the FIB subsystem and the DBE in cases where the latter is located at the central facility (could be the case for the SBA).

Parameter	Req. #	Value	Traceability
Network Latency	CSP1038	The CSP shall support data transport delays of up to 250 ms with no additional correlation loss.	[AD28] SYS0502
Packet-Loss Tolerance	CSP1039	The CSP shall be tolerant of packet loss in communication of data from the antennas.	[AD28]
CSP Input Data Physical Interface	CSP1040	The CSP physical interface with FIB shall follow the specifications in [AD28].	[AD28]

The System Requirements' goal of connecting to other flagship capabilities states, "A minimum capability would provide the requisite delay buffers to accommodate the projected network delays to the GBT. A more capable implementation would have delay buffers to interface with Effelsberg and phased ALMA." Specific network latency required is still under assessment.



Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

It is anticipated that the communication links from the antennas may incur in data loss, particularly in long-distance links using third-party infrastructure. The CSP shall be tolerant of this data loss, meaning that it must be integrated into operation, by monitoring and reporting such events as will be determined in the future. CSP performance, however, will be impacted by data loss.

7.2.10 020.10.40.05.00-0122 DBE–Antenna Time and Frequency Interface Requirements

The DBE uses an external time and frequency reference to generate its internal clock and data timestamps. Additionally, some data processing tasks are performed at specific time events. This interface defines the mechanical and electrical interface through which the DBE acquires the external time and frequency references from the Antenna Time and Frequency subsystem (ATF, CI number 020.30.35.00.00).

Parameter	Req. #	Value	Traceability
DBE Timing Interface	CSP1041	The DBE time reference input shall follow the specifications in [AD29].	[AD29]
DBE External Frequency Interface	CSP1042	The DBE frequency reference input shall follow the specifications in [AD29].	[AD29]

7.2.11 020.10.40.05.00-0123 CSP–LO Reference & Timing Generation Interface Requirements

The CSP at the central facility employs external time and frequency references that are internally distributed to every device that needs them to generate their internal clock and data timestamps. Some data processing tasks are performed at specific time events. This interface defines the mechanical and electrical interface through which the CSP acquires the external time and frequency references from the LO Reference & Timing Generation subsystem (RTG, CI number 020.35.05.00.00).

Parameter	Req. #	Value	Traceability
CSP Timing Interface	CSP1043	The CSP time reference input shall follow the specifications in [AD30].	[AD30]
CSP External Frequency Interface	CSP1044	The CSP frequency reference input shall follow the specifications in [AD30].	[AD30]

7.3 Safety and Security Requirements

This section defines all design requirements necessary to support the Level-I Safety, Security and Cybersecurity requirements derived from [AD03], [AD07], and [AD08].

Parameter	Req. #	Value	Traceability
Safety Specification	CSP2001	The CSP shall comply with Safety Specifications [AD07].	[AD07] SYS2700
Security Specification	CSP2002	The CSP shall comply with Security Plan and Requirements [AD08].	[AD08] SYS2703
Cybersecurity Specification	CSP2003	The CSP shall be engineered and deployed in accordance with current best practices in IT Security, as defined by the NSF-funded Center for Trustworthy Scientific Infrastructure and the AUI Cyber Security Policy.	SYS2702



Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

7.4 Reliability, Availability, and Maintainability Requirements

This section defines all RAM requirements and Logistic Support requirements derived from [AD03].

Parameter	Req. #	Value	Traceability
Safe Restart	CSP3001	All CSP sub-elements shall restore the Standby (Default) Mode in the event of network or power outages, or after a full power cycle, without human intervention.	SYS2304 SYS3114
Modularization	CSP3002	The CSP shall be modularized into Line Replaceable Units (LRUs) to facilitate site maintenance.	SYS2403
Self-Diagnostic Function	CSP3003	All CSP sub-elements shall incorporate self-diagnosis functions to identify faults based on recorded monitor data.	SYS2405
Configuration Monitoring	CSP3004	The CSP shall include monitoring and tracking of its configuration to the LRU level.	SYS2406
Engineering Console	CSP3005	The CSP shall include an engineering console to communicate system status and assist in real-time diagnosis at the LRU level.	SYS2407
Monitor Variable Data Rate	CSP3006	The CSP shall stream monitor data at variable rates (0.1 sec to 10 min) for automated use by predictive maintenance programs and for direct inspection by engineers and technicians.	SYS2408 SYS2409
Spares Planning	CSP3007	Failure analysis shall be used in the planning of spares inventory. Factors considered shall include the projected availability for spares, the time required to repair the failure, and the viability of critical vendors.	SYS3204
Operations and Maintenance: Transfer of Deliverables	CSP3008	All procedures, test equipment, and test software shall be delivered to the Operations and Maintenance staff prior to full operations.	SYS3211
Remote Updates	CSP3009	The CSP shall permit the update of individual LRU firmware and software to be performed remotely via a network connection.	SYS3223
Local Control	CSP3010	Local control of the antenna sub-elements shall not depend on the availability of remotely accessed networked systems.	SYS3224
LRU Monitoring	CSP3011	All CSP LRUs shall provide on-board monitoring and diagnostics to determine the health and status of the unit.	SYS2701 SYS3101
Automated Failure Reporting	CSP3012	The Self-Diagnostic Function shall automatically log issues to the issue tracking database via the M&C system.	SYS3102 SYS3225 SYS3235 SYS3238
LRU Interchangeability	CSP3013	LRUs should be interchangeable with no on-site calibration, tuning, or alignment.	SYS3232



Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

Parameter	Req. #	Value	Traceability
Electronic Identification	CSP3014	All LRUs shall have electronically identifiable (Bar Code, RFID tag or similar) Part Marking as defined in the Configuration Management Plan.	SYS3233
Identify Failures Physically	CSP3015	All LRUs shall identify a failed state via physical display (e.g., LED).	SYS3234
Report Predicted Failures	CSP3016	All LRUs, where possible, shall report fault prediction sensor data via the M&C system.	SYS3236
Failure Information Source	CSP3017	All LRUs shall report failure information in line with failure isolation as identified in a FMECA analysis.	SYS3237
Fast Read-Out Modes	CSP3018	Fast read-out modes shall be available for remote engineering diagnostics of all LRUs (i.e., an on-board oscilloscope function).	SYS3105
Hot Swaps of LRUs	CSP3019	The CSP shall be designed to accommodate and recover from hot swaps with minimal human interaction.	SYS3111
CSP Availability and Reliability	CSP3020	The CSP MTBF shall exceed TBD hours; with an MTTR less than TBD hours.	SYS2601 SYS2602 SYS2605 [AD10]
Preventive Maintenance	CSP3021	The CSP shall not require down time due to preventive maintenance. All preventive maintenance of the CSP shall be done while the CSP is operational, without interrupting observations.	SYS2603
EMI/RFI Compliance	CSP3022	Superseded by Section 7.2.6.	
DBE Mean Time Between Maintenance	CSP3023	The DBE MTBM shall exceed 20,000 hours.	SYS2610

CSP3020 will be determined once the corresponding system technical budget to satisfy the Telescope Inherent Availability defined in SYS2605 is specified.

The intent of CSP3021 is to require that preventive maintenance be done on a reduced number of LRUs, which can be taken out of operation during maintenance, while the rest of the CSP equipment remains operational. Additional sub-elements (e.g., SBP Units) may be installed as needed to guarantee minimum operational capabilities during maintenance.



Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

7.5 Configuration and Document Management Requirements

This section defines Configuration Management requirements and Documentation requirements, derived from [AD03].

Parameter	Req. #	Value	Traceability
Serial Numbers	CSP4001	All configuration items (e.g., LRUs) shall be uniquely identifiable to facilitate status and location tracking across the Observatory. Identification for LRUs shall be both visible and electronic.	SYS3600
Version Control	CSP4002	All custom software and firmware delivered as part of the system shall be version controlled via a configuration management process.	SYS3602
Configuration Retrieval	CSP4003	All configurable LRUs shall retrieve their hardware parameter configuration automatically after installation.	SYS3603
As-Built Drawings	CSP4004	As-built drawings shall be provided for all custom hardware and facilities delivered as part of the system.	SYS6001
Operations and Maintenance Manuals	CSP4005	Operations and Maintenance Manuals shall be provided for each LRU in the system.	SYS6002
Units	CSP4006	Design materials and documentation shall use SI (metric) units.	SYS6003
Language	CSP4007	The language used for written documentation shall be English.	SYS6004
Electronic Document Format	CSP4008	Native, editable file formats of all documents and drawings of record shall be delivered, along with their PDF versions.	SYS6005

7.6 Life Cycle Requirements

This section defines the System Life Cycle requirements, including design and development, AIV, and CSV as derived from [AD03].

Parameter	Req. #	Value	Traceability
Design Life	CSP5001	The CSP shall be designed for an expected operational life of no less than 30 years.	SYS2801
Cost Optimization	CSP5002	The CSP shall be designed to minimize total life-cycle costs over the projected design life, extending through system decommissioning/disposal.	SYS2802
Sustainability	CSP5003	Sustainability and long-term environmental impact shall be considered in any material or design trade-study.	SYS2803
Part Selection for Maintainability	CSP5004	Individual component selection criteria shall include the projected continuity of support for the component or interchangeable equivalents over the system design life.	SYS2805



Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

Parameter	Req. #	Value	Traceability
Critical Spares	CSP5005	CSP critical spares shall be identified and provided with sufficient inventory to support the facility for its operational life (CSP5001).	SYS2812
Packaging Supply	CSP5006	When applicable, shipping cases and packaging for transportation and storage of CSP elements in compliance with CSP9001 and CSP9002 shall be provided.	SYS3904 SYS3905 SYS3912
Quality Control of Deliverables	CSP5007	Stand-alone acceptance testing of software and hardware deliverables shall occur before delivery and installation on the array.	SYS3702
Test Fixtures	CSP5008	Test fixtures and procedures shall be provided for CSP level verification.	SYS2811
Testing of Software and Firmware	CSP5009	All software and firmware shall be delivered with automated unit, integration, and regression testing suites.	SYS2814
AIV Software Tools	CSP5010	Development tools, compilers, source code, and the build system shall be delivered to enable maintenance over the life of the facility.	SYS2815
Electronics Specifications	CSP5011	All electronic components of the CSP shall be designed, manufactured, assembled, manipulated, shipped, installed, and maintained in compliance with System Electronics Specifications [AD09].	[AD09]
ICD LRUs	CSP5012	ICDs shall be delivered for each CSP LRU.	SYS2818
Incremental Delivery to Operations	CSP5013	Operational capabilities and modes shall be made available in stages during the transition from construction to full operations.	SYS2830

In System Requirements [AD03], operational life is defined to start at the full operations milestone and close-out of the construction project, and SYS2801 sets a duration of 20 years. However, the operational life of the SCP is defined to start with construction and commissioning activities, 10 years ahead of full operations.

Critical spares are defined as parts that are likely to be obsoleted over the operating life, are unlikely to have market substitutes, and cannot be produced/ordered in small volumes.



Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

8 Key Performance Parameters (KPPs)

Key Performance Parameters (KPPs) identify critical subsystem capabilities or characteristics that may either have a detrimental impact on the effectiveness of efficiency of the system if not met, or could have a very large positive impact if the specification is exceeded. Subsystem KPPs typically support System KPPs and there should be traceability between them. Each KPP must have a threshold range and objective value. The responsible engineer designs the subsystem to meet the objective value, but performance within the threshold range is considered acceptable. During the design phase, there should be a concerted effort to optimize the KPPs. If the responsible engineer finds that the minimum threshold level of a KPP cannot be achieved the project office shall be notified immediately.

Key Performance Parameter	Req. #	Traceability LI Req. #
KPP name / description: Subarray Independence Objective value: Full independence Threshold range: Table I of System Requirements [AD03]	CSP0019	SYS0606 SYS0608
KPP name / description: Availability Objective value: TBD Threshold range: TBD	CSP3023	SYS2601 SYS2602 SYS2605 [AD10]
KPP name / description: Longest Baseline Objective value: 8800 km Threshold range: 8800 km and above	CSP0057	SYS1301
KPP name / description: Per-Antenna Available Bandwidth Objective value: 20 GHz Threshold range: 14 GHz and above	CSP0058	SYS0903
KPP name / description: Number of frequency channels Objective value: 1,288,000 Threshold range: 240,000 and above	CSP0059	SYS1402
KPP name / description: Interferometric Frequency Resolution Objective value: 250 Hz Threshold range: 1 kHz and below	CSP0060	SYS1401
KPP name / description: Interferometric Time Resolution Objective value: 1 ms to 5 s Threshold range: 100 ms to 5 s	CSP0061	SYS0106

Table 2: Subsystem Key Performance Parameters.

Many CSP requirements are critical in the sense that the System relies solely on the CSP to satisfy a requirement. Therefore, if not met, they would have a significant impact on the system effectiveness. Nevertheless, they have not been included as KPP as their satisfaction is not deemed at risk, and they do not support any system KPP. Future revisions may include additional KPPs based on updated risk assessment.



Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

9 Verification

The design will be verified to meet the requirements by analysis (A), inspection (I), demonstration (D), or test (T), each defined below.

Verification by Analysis: The compliance of the subsystem to the requirement is demonstrated by appropriate analysis (hand calculations, finite element analysis, modeling and simulation, etc.).

Verification by Inspection: The compliance of the subsystem to the requirement is determined by a simple inspection of the subsystem or of its design documentation.

Verification by Demonstration: The compliance of the subsystem to the requirement is determined by a demonstration.

Verification by Test: The compliance of the subsystem to the requirement is determined by means of a test with and associated analysis of test data.

Multiple verification methods are allowed over the course of the design phase. The primary (final) verification method to be used for the product during the qualification phase prior to its Critical Design Review is identified below.

9.1 Verification Methods

9.1.1 Functional and Performance Requirements

Req. #	Parameter/Requirement	A	I	D	T
CSP0001	Interferometric Capabilities		*		
CSP0002	Beamforming Capabilities		*		
CSP0003	Transient Analysis Capabilities		*		
CSP0004	Reconfiguration Time	*			*
CSP0005	Standby Mode		*		
CSP0006	Connected Antennas		*		
CSP0007	Polarization		*		
CSP0008	Per-Antenna Available Bandwidth		*		
CSP0009	Correlation Loss	*			*
CSP0010	Longest Baseline		*		
CSP0011	Number of frequency channels		*		
CSP0012	Timing Accuracy		*		
CSP0013	Polarization Dynamic Range		*		
CSP0014	Commensal Signal Processors		*		
CSP0015	Self-Generated Spurious Signal Power Level	*			*
CSP0016	Subarray Operation		*		
CSP0017	Number of Subarrays		*		
CSP0018	Simultaneous Subarray Capabilities		*		
CSP0019	Subarray Independence		*	*	
CSP0020	Subarray Reconfiguration		*	*	
CSP0021	Interferometric Bandwidth		*		
CSP0022	Interferometric Frequency Resolution		*		
CSP0023	Interferometric Variable Frequency Resolution		*		
CSP0024	Interferometric Time Resolution		*		
CSP0025	Interferometric Channel Flatness		*		



Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

Req. #	Parameter/Requirement	A	I	D	T
CSP0026	Interferometric Frequency Selectivity	*			
CSP0027	Interferometric Polarization Products		*		
CSP0028	Beamformer Aperture		*		
CSP0029	Number of Beams		*		
CSP0030	Beamformer Bandwidth per Beam		*		
CSP0031	Beamformer Field of View		*		
CSP0032	Beamforming SNR Efficiency	*			*
CSP0033	Beamformer Polarization Correction		*		
CSP0034	Concurrent Interferometric Mode		*		
CSP0035	VLBI Support		*		
CSP0036	Transient Stokes Parameters		*		
CSP0037	Dedispersion and Folding Capabilities		*		
CSP0038	Transient Analysis Bandwidth		*		
CSP0039	Transient Analysis Number of Beams		*		
CSP0040	Transient Analysis Time Resolution		*		
CSP0041	Transient Analysis Frequency Resolution		*		
CSP0042	Transient Analysis SNR Efficiency	*			
CSP0043	Sideband Separation		*		
CSP0044	Sub-band Generation		*		
CSP0045	Sub-band Selection		*		
CSP0046	Sub-band Bandwidth		*		
CSP0048	LO Offset Support		*		
CSP0049	RFI Mitigation		*		
CSP0050	Geometric Delay		*		
CSP0051	Delay and Phase Tracking Update Rate		*		
CSP0052	Sampler Clock Offset Support		*		
CSP0053	Delay and Phase Tracking SNR Loss		*		
CSP0054	Dispersion Measure Range		*		
CSP0055	Pulse Profile Bins		*		
CSP0056	Pulse Period		*		
CSP0057	Sideband Separation Level	*			
CSP0058	Secondary Subarray Capabilities			*	

9.1.2 Interface Requirements

Req. #	Parameter/Requirement	A	I	D	T
CSP1001	Deterministic Input Data Buffer Latency			*	
CSP1002	IRD Data BER				*
CSP1003	IRD Data Integrity				*
CSP1004	IRD Data Clock Recovery				*
CSP1005	IRD Data Modulation			*	
CSP1006	IRD Data FEC Encoding			*	
CSP1007	IRD Data Deserialization			*	
CSP1008	IRD Data Format			*	
CSP1009	DBE Power Interface		*		
CSP1011	DBE Safety Monitoring				*
CSP1012	DBE Dimensions				*



Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

Req. #	Parameter/Requirement	A	I	D	T
CSPI013	DBE Thermal Load				*
CSPI014	DBE RFI Emissions				*
CSPI015	DBE Fastening		*		
CSPI016	DBE M&C Physical Interface		*		
CSPI017	DBE Monitor Data Rate				*
CSPI018	DBE Configuration Data Rate				*
CSPI019	DBE Monitor Parameters			*	
CSPI020	DBE Configuration Protocol			*	
CSPI021	DBE Fiber Interface		*		
CSPI022	DBE Input Data Rate			*	
CSPI023	DBE Output Data Rate			*	
CSPI025	CSP Safety Monitoring				*
CSPI026	CSP Dimensions		*		
CSPI027	CSP Thermal Load				*
CSPI028	CSP RFI Emissions				*
CSPI029	CSP Fastening		*		
CSPI030	Backup Power Operation			*	
CSPI031	CSP M&C Physical Interface		*		
CSPI032	CSP Configuration Data Rate				*
CSPI033	CSP Monitor Parameters			*	
CSPI034	CSP Configuration Protocol			*	
CSPI035	CSP Data Physical Interface		*		
CSPI036	CSP Output Data Rate				*
CSPI037	CSP Output Data Format			*	
CSPI038	Network Latency			*	
CSPI039	Packet-Loss Tolerance			*	
CSPI040	CSP Input Data Physical Interface		*		
CSPI041	DBE Timing Interface			*	
CSPI042	DBE External Frequency Interface			*	
CSPI043	CSP Timing Interface			*	
CSPI044	CSP External Frequency Interface			*	
CSPI045	CSP Immunity				*
CSPI046	CSP Normal Operation Temperature				*
CSPI047	CSP Normal Operation Relative Humidity				*
CSPI048	DBE Normal Operation Temperature				*
CSPI049	DBE Normal Operation Relative Humidity				*
CSPI050	CSP Maximum Power Consumption				*

9.1.3 Safety and Security Requirements

Req. #	Parameter/Requirement	A	I	D	T
CSP2001	Safety Specification			*	
CSP2002	Security Specification			*	
CSP2003	Cybersecurity Specification			*	



Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

9.1.4 Reliability, Availability, and Maintainability Requirements

Req. #	Parameter/Requirement	A	I	D	T
CSP3001	Safe Restart			*	
CSP3002	Modularization		*		
CSP3003	Self-Diagnostic Function			*	
CSP3004	Configuration Monitoring			*	
CSP3005	Engineering Console			*	
CSP3006	Monitor Variable Data Rate			*	
CSP3007	Spares Planning	*			
CSP3008	Operations and Maintenance: Transfer of Deliverables				
CSP3009	Remote Updates			*	
CSP3010	Local Control			*	
CSP3011	LRU Monitoring			*	
CSP3012	Automated Failure Reporting			*	
CSP3013	LRU Interchangeability			*	
CSP3014	Electronic Identification		*		
CSP3015	Identify Failures Physically			*	
CSP3016	Report Predicted Failures	*			
CSP3017	Failure Information Source			*	
CSP3018	Fast Read-Out Modes			*	
CSP3019	Hot Swaps of LRUs			*	
CSP3020	CSP Availability and Reliability	*			
CSP3021	Preventive Maintenance			*	
CSP3023	DBE Mean Time Between Maintenance	*			

9.1.5 Configuration and Document Management Requirements

Req. #	Parameter/Requirement	A	I	D	T
CSP4001	Serial Numbers		*		
CSP4002	Version Control		*		
CSP4003	Configuration Retrieval		*		
CSP4004	As-Built Drawings		*		
CSP4005	Operations and Maintenance Manuals		*		
CSP4006	Units		*		
CSP4007	Language		*		
CSP4008	Electronic Document Format		*		

9.1.6 Life Cycle Requirements

Req. #	Parameter/Requirement	A	I	D	T
CSP5001	Design Life	*			
CSP5002	Cost Optimization	*			
CSP5003	Sustainability	*			
CSP5004	Part Selection for Maintainability		*		
CSP5005	Critical Spares		*		
CSP5006	Packaging Supply		*		
CSP5007	Quality Control of Deliverables		*		
CSP5008	Test Fixtures		*		



Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

Req. #	Parameter/Requirement	A	I	D	T
CSP5009	Testing of Software and Firmware		*		
CSP5010	AIV Software Tools		*		
CSP5011	Electronics Specifications		*		
CSP5012	ICD LRUs		*		
CSP5013	Incremental Delivery to Operations		*		

9.1.7 Environmental Requirements

Req. #	Parameter/Requirement	A	I	D	T
CSP9001	Packaging for Transportation		*		
CSP9002	Packaging for Storage		*		
CSP9003	Altitude Range			*	
CSP9004	Seismic Protection				*
CSP9005	Vibration protection				*
CSP9007	General Vibration				*
CSP9008	Mechanical Shocks				*

9.2 Verification Requirements

Req. #	Parameter/Requirement	Verification Requirement
CSP0004	Reconfiguration Time (Analysis)	A reconfiguration flowchart and timing diagram showing compliance shall be provided.
CSP0004	Reconfiguration Time (Test)	The reconfiguration time for a predefined set of use cases shall be measured after CSP subsystem integration.
CSP0009	Correlation Loss (Analysis)	CSP Performance Analysis shall include a calculation of the correlation loss.
CSP0009	Correlation Loss (Test)	The correlation loss of the CSP for a predefined set of use cases shall be measured after CSP subsystem integration.
CSP0015	Self-Generated Spurious Signal Power Level (Analysis)	CSP Performance Analysis shall include a calculation of the self-generated spurious signal power level.
CSP0015	Self-Generated Spurious Signal Power Level (Test)	The self-generated spurious signal power level of the CSP for a predefined set of use cases shall be determined by simulation.
CSP0026	Interferometric Frequency Selectivity	CSP Performance Analysis shall include a calculation of the interferometric frequency selectivity.
CSP0032	Beamforming SNR Efficiency (Analysis)	CSP Performance Analysis shall include a calculation of the beamforming SNR efficiency.
CSP0032	Beamforming SNR Efficiency (Test)	The beamforming SNR efficiency of the CSP for a predefined set of use cases shall be measured after CSP subsystem integration.
CSP0042	Transient Analysis SNR Efficiency	CSP Performance Analysis shall include a calculation of the transient SNR efficiency.
CSP0047	Sub-band Selection Reconfiguration Time	A reconfiguration flowchart and timing diagram showing compliance shall be provided.
CSP1014	DBE RFI Emissions	Test as per [AD05].



Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

Req. #	Parameter/ Requirement	Verification Requirement
CSP1028	CSP RFI Emissions	Test as per [AD05].
CSP1050	CSP Maximum Power Consumption	Power consumption characterization in normal operation conditions
CSP9005	Vibration Protection	All three axes as defined in the MIL-STD-810H Method 514.8 Procedure I for General Vibration, for a period of 60 minutes
CSP9007	Transportation Vibration Protection	All three axes as defined in the MIL-STD-810H Method 514.8 Procedure I for General Vibration, for a period of 60 minutes
CSP9008	Mechanical Shocks	MIL-STD-810H Method 516.8 Logistic Transit Drop Test



Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

10 Appendix

10.1 Abbreviations and Acronyms

Acronym	Description
AD	Applicable Document
AIV	Acceptance, Integration, and Verification
ARCS	Advanced RF Containment System
ATF	Antenna Time and Frequency
BER	Bit Error Rate
BMR	Bins, Modules and Racks
CSP	Central Signal Processor
CSS	Computing and Software System
DBE	Digital Back End
EIRP	Effective Isotropic Radiated Power
EMI	Electromagnetic Interference
FEC	Forward Error Correction
FIB	Central Fiber Optic Distribution / Central Fiber Infrastructure
FMECA	Failure Mode, Effects & Criticality Analysis
FRACAS	Failure Reporting, Analysis, and Corrective Action System
ICD	Interface Control Document
IRD	Integrated Receivers and Digitizers
KPP	Key Performance Parameter
LBA	Long Baseline Array
LO	Local Oscillator
LRU	Line Replaceable Unit
M&C	Monitor & Control
MTBF	Mean Time Between Failures
MTBM	Mean Time Between Maintenance
MTTR	Mean Time to Repair or Replace
ngVLA	Next Generation Very Large Array
NSB	ngVLA Site Buildings
NRAO	National Radio Astronomy Observatory
ONL	Online Sub-Element
OTF	On the Fly
PDR	Preliminary Design Review
PSE	Pulsar Engine
RD	Reference Document
RF	Radio Frequency
RFI	RF Interference
RTD	LO Reference and Timing Distribution
RTG	LO Reference and Timing Generation
SBA	Small Baseline Array
SBP	Sub-Band Processor
SNR	Signal-to-Noise Ratio
TBC	To Be Confirmed
TBD	To Be Determined



Title: Central Signal Processor Requirements Specification	Owner: O. Yeste Ojeda	Date: 2022-02-10
NRAO Doc. #: 020.40.00.00.00-0001-REQ		Version: B

Acronym	Description
VDIF	VLBI Data Interchange Format
VLB	Very Long Baseline
VLBI	VLBI Interferometry











020.40.00.00.00-0001-REQ-B-CSP_REQUIREMENTS-CoDR

Final Audit Report


2022-02-11

Created:	2022-02-11
By:	Anne Lear (alear@nrao.edu)
Status:	Signed
Transaction ID:	CBJCHBCAABAAKswgspcsRclj4dSyAZhNCeYIn0vYE6iU


"020.40.00.00.00-0001-REQ-B-CSP_REQUIREMENTS-CoDR" History

-  Document created by Anne Lear (alear@nrao.edu)
2022-02-11 - 3:33:43 AM GMT- IP address: 75.161.242.227
-  Document emailed to William Shillue (bshillue@nrao.edu) for signature
2022-02-11 - 3:35:02 AM GMT
-  Email viewed by William Shillue (bshillue@nrao.edu)
2022-02-11 - 1:36:38 PM GMT- IP address: 192.131.232.128
-  Document e-signed by William Shillue (bshillue@nrao.edu)
Signature Date: 2022-02-11 - 1:37:06 PM GMT - Time Source: server- IP address: 192.131.232.128
-  Document emailed to R. Selina (rselina@nrao.edu) for signature
2022-02-11 - 1:37:09 PM GMT
-  Email viewed by R. Selina (rselina@nrao.edu)
2022-02-11 - 2:01:34 PM GMT- IP address: 75.161.226.40
-  Document e-signed by R. Selina (rselina@nrao.edu)
Signature Date: 2022-02-11 - 3:33:11 PM GMT - Time Source: server- IP address: 75.161.226.40
-  Document emailed to Thomas Kusel (tkusel@nrao.edu) for signature
2022-02-11 - 3:33:13 PM GMT
-  Email viewed by Thomas Kusel (tkusel@nrao.edu)
2022-02-11 - 5:06:30 PM GMT- IP address: 71.62.226.171
-  Document e-signed by Thomas Kusel (tkusel@nrao.edu)
Signature Date: 2022-02-11 - 5:07:11 PM GMT - Time Source: server- IP address: 71.62.226.171




 Document emailed to Willem Esterhuyse (westerhu@nrao.edu) for signature

2022-02-11 - 5:07:13 PM GMT

 Email viewed by Willem Esterhuyse (westerhu@nrao.edu)

2022-02-11 - 5:08:24 PM GMT- IP address: 105.224.252.103

 Document e-signed by Willem Esterhuyse (westerhu@nrao.edu)

Signature Date: 2022-02-11 - 5:09:17 PM GMT - Time Source: server- IP address: 105.224.252.103

 Agreement completed.

2022-02-11 - 5:09:17 PM GMT

