Integrated Downconverters and Digitizers Design Description

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PREPARED BY	ORGANIZATION	DATE
M. Morgan	Electronics Div., NRAO	2018-11-01
S. Durand, Antenna Electronics IPT Lead	Electronics Div., NRAO	2019-04-12

APPROVALS (Name and Signature)	ORGANIZATION	DATE
R. Selina, Project Engineer R Selina 2019.07.25 12:37:44 -06'00'	Electronics Div., NRAO	2019-07-25
M. McKinnon, Project Director Mark McKinnon Digitally signed by Mark McKinnon Date: 2019.07.25 16:16:30 -06'00'	Asst. Director for NM-Operations, NRAO	2019-07-25

RELEASED BY (Name and Signature)	ORGANIZATION	DATE
M. McKinnon, Project Director Mark McKinnon Digitally signed by Mark McKinnon Date: 2019.07.25 16:16:52 -06'00'	Asst. Director for NM-Operations, NRAO	2019-07-25

Change Record

Version	Date	Author	Affected Section(s)	Reason
1	2018-03-13	M. Morgan	All	Initial Draft, based on template provided.
2	2018-03-29	M. Morgan	5.1–5.3	Modified LO frequencies for Band 5.
3	2018-04-16	M. Morgan	4, 5.1, 5.2.3, 5.3.4	Removed references to thermoelectric coolers.
4	2018-04-26	M. Morgan	Many	Increased to 8 bits in Bands 4 and 5, and added two Band 4 modules for WVR. Added 3.3 V digital supply.
5	2018-05-24	M. Morgan	Header	Corrected file number.
6	2018-06-26	M. Morgan	Header	Recorrected file number.
7	2018-07-03	M. Morgan	Fig. 2	Corrected Band 2 edge frequencies.
8	2018-09-06	S. Durand	All	Minor changes.
9	2018-09-25	M. Morgan	5.2.1	Clarified that cooling fans on the pictured prototype will not be present in reference design version.
A	2019-07-25	A. Lear	All	Prepared PDF for approvals and release.

Table of Contents

1 Introduction

1.1 Purpose

This document provides a description for the Integrated Downconverters and Digitizers subsystem reference design. It covers the design approach, functions, description of key components, interfaces, and risks associated with the reference design. This document will form part of the submission of the ngVLA Reference Design documentation package.

1.2 Scope

The scope of this document covers the entire design of the Integrated Downconverters and Digitizers subsystem, as part of the ngVLA Reference Design. It includes the subsystem's design, how it functions, and interfaces with the necessary hardware and software systems. It does not include specific technical requirements or budgetary information.

2 Related Documents and Drawings

2.1 Applicable Documents

The following documents may not be directly referenced herein, but provide necessary context or supporting material.

Ref. No.	Document Title	Rev/Doc. No.
AD01	Integrated Receivers and Downconverters Preliminary Technical Specifications/Requirements	020.30.15.00.00-0001-REQ

2.2 Reference Documents

The following documents are referenced within this text:

Ref. No.	Document Title	Rev/Doc. No.
RD01	Experiments With Digital Sideband-Separating Downconversion	M. Morgan and J. Fisher, *Publications of the Astronomical Society of the Pacific*, vol. 122, no. 889, pp. 326–335, March 2010.
RD02	Unformatted Digital Fiber-Optic Data Transmission for Radio Astronomy Front Ends	M. Morgan, J. Fisher, and J. Castro, *Publications of the Astronomical Society of the Pacific*, vol. 125, no. 928, pp. 695–704, June 2013.
RD03	A highly-sensitive cryogenic phased array feed for the Green Bank Telescope	D. Roshi, W. Shillue, J. Fisher, M. Morgan, J. Castro, W. Groves, T. Boyd, B. Simon, L. Hawkins, V. van Tonder, J. Nelson, J. Ray, T. Chamberlain, S. White, R. Black, K. Warnick, B. Jeffs, and R. Prestage, 32nd URSI General Assembly and Scientific Symposium, Montreal, August 2017.
RD04	SO-QSFP28-PAM4-Dxxx datasheet	https://www.smartoptics.com/wp-content/uploads/2017/10/SO-QSFP28-PAM4-DWDM-R4.0.pdf
RD05	Eoptolink 200G-400G solutions	http://www.eoptolink.com/200g-400g

3 Subsystem Overview

The Integrated Receiver and Digitizer (IRD) packages further amplify the signals provided by the cryogenic stage, downconvert them where necessary, digitize them, and deliver the resultant data streams by optical fiber to a moderately remote collection point from the focal plane (but possibly still inside the antenna base). From there, they can be time-stamped and launched onto a more conventional network for transmission back to the array correlator and central processing facility. Hooks are needed to provide for synchronization of local oscillators (LOs) and sample clocks, power leveling, command and control, health and performance monitoring, and diagnostics for troubleshooting in the event of component failure.

This subsystem consists of direct-sampled and sideband-separating modules for all telescope bands, which include warm amplification, filtering, power leveling, analog-to-digital conversion, and fiber-optic transmission. It also includes external splitters and combiners as needed to feed them from the cryogenic signal paths. Cryogenic systems and thermal transitions, as well as front-end cabling, waveguide runs, and fiber-optic signal paths outside the IRD modules themselves, are outside the scope of this work package, though interfaces must be considered.

4 Subsystem Design

The design of the ngVLA IRD modules evolved from an internal research program (the Integrated Receiver Development program), which has been perfecting the techniques used in their construction for more than a decade at the time of this writing. The original program aimed to leverage the advantages of modern electronic integration and digital signal processing, to digitize as closely to the antenna feed-point as possible without comprising ultimate performance, and to re-optimize legacy receiver architectures in light of these new techniques and in anticipation of future telescope facilities such as the ngVLA.

Integration and digital signal processing (DSP) are deemed complementary in this program, in that the latter provides for greater signal fidelity and precision in concert with detailed calibrations than purely analog techniques, while the former guarantees the long-term stability and uniformity of those calibrations. This resulted also in compact, low-power, field-replaceable receiver units which were a perfect fit for ngVLA's maintenance and operability requirements.

Paramount to the integrated receiver subsystem design is coverage of all operating bands on the telescope with the minimum number of discrete integrated modules. This minimizes construction, testing, operating, and maintenance costs as well as reducing the complexity of the data transport and timing distribution subsystems. The limiting factor here is digitizer bandwidth and sample rate. The ngVLA has a requirement to digitize instantaneously 20 GHz of bandwidth, with a goal of sampling the entire frequency range of any given RF band simultaneously (Band 6 in particular covering more than 20 GHz of bandwidth). This is more than can be sampled instantaneously at the bit depth required with a single analog-to-digital converter (ADC) having reasonable performance and power dissipation. Thus, the system will consist of low-loss splitters following the cryogenic front-end feeding a number of integrated receiver modules in parallel.

Due to the compact, integrated construction, it is unwise to perform downconversion in multiple steps. Integrated modules, though they have many advantages, do not typically have as good of isolation between inputs as individually connectorized components. Multiple local oscillator tones, then, tend to produce a copious spread of mixing products that inevitably lead to spurious tones in the output spectrum.

We therefore process the higher frequency bands using a single-stage, direct-to-baseband downconversion with in-phase and quadrature (I and Q) channels. These channels are then processed

numerically in the back-end to produce upper and lower sidebands more precisely than an analog hybrid ever could. The IRD program has a long track record of producing clean output spectra with 50–60 dB sideband suppression using this technique (e.g. [RD01]).

At the lower frequency bands, downconversion is an unnecessary complexity, usually requiring triple-balanced mixers to achieve the required IF bandwidth while isolating it from the RF and LO inputs which overlap with it in frequency space. For these bands, instead, we use a direct-digitization approach in the second or third Nyquist-zone of the sampler.

To minimize power requirements and the risk of self-interference with integrated digital and high-gain analog electronics, the IRD program developed a novel approach to digital data transmission. Specifically, it delivers unformatted digital data streams over optical fiber without any of the usual bit-scrambling, packetizing, or formatting (e.g. 8b/10b) used in the data-communications industry. This "low-overhead" digital design [RD02] relies on the statistical characteristics of Gaussian-distributed white noise—which dominates the signal in any properly designed radio astronomy receiver, even those heavily laced with man-made interference—to parse the bit stream at the receive-end of the fiber, away from the focal plane where power and interference are less harmful. Numerous demonstrations of this concept have been built and proven, and it has now been fielded in a user instrument on the Green Bank Telescope [RD03].

A critical element of the low-overhead serial link described above is the Serial ADC (SADC). This essentially marries a conventional ADC and a conventional Serializer (or SerDes) without any of the usual, intervening, complex digital logic. Implemented to date using off-the-shelf parts, fully realizing this idea's potential benefits relies on integrating these two components on a single piece of Silicon. This avoids the wasted size, weight, and power (SWaP) associated with chip-to-chip parallel interfaces. The functional components of this proven technique (the ADC and the Serializer) already exist commercially, making this a development with very low technical risk, but one that requires a significant investment in producing the ASIC. Such a development has been initiated with a contract IP vendor. The projected power dissipation of this chip is 25 times less than that consumed by off-the-shelf solutions.

The unformatted fiber optic links will likely not interface directly with the array correlator/signal processor. Rather, they will interface with the long-distance data transmission subsystem which will carry the data the rest of the way on more conventional (possibly commercial) links. The data transmission subsystem interface could be inside the antenna base or some tens of kilometers away where it will join with links from other telescopes in the array. The latter will most likely be the case at least for the antennas in the array core within reach of the signal processing center.

4.1 Subsystem Block Diagram

A block diagram of the Integrated Receivers/Downconverters and Digitizers Subsystem is shown in Figure 1, with all electrical interfaces included. The internal block diagrams of the sideband separating (2SB) and direct-sampled (DS) receiver modules appear in Section 4.2. The gray boxes provide information about subsystem inputs and outputs.

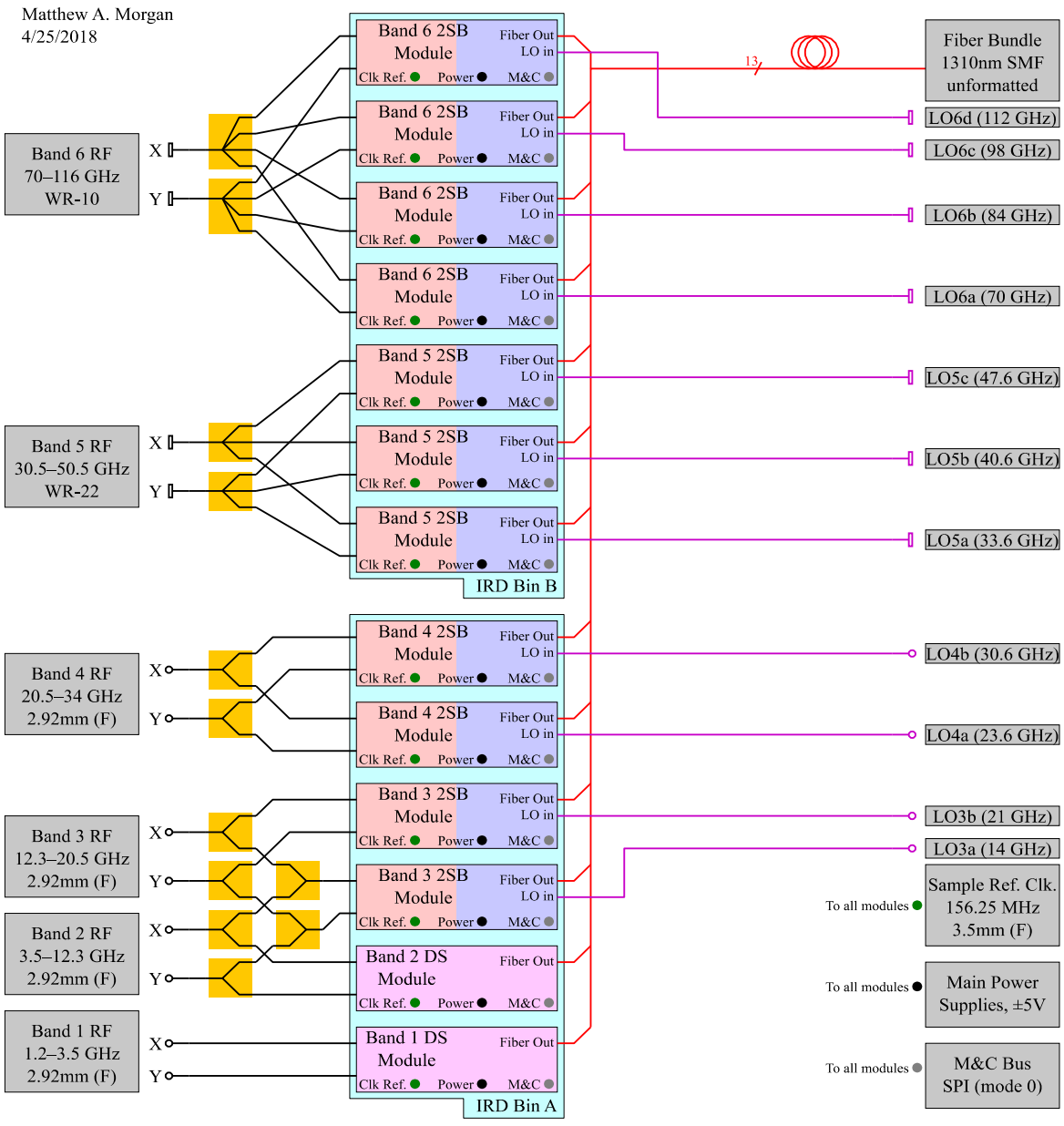
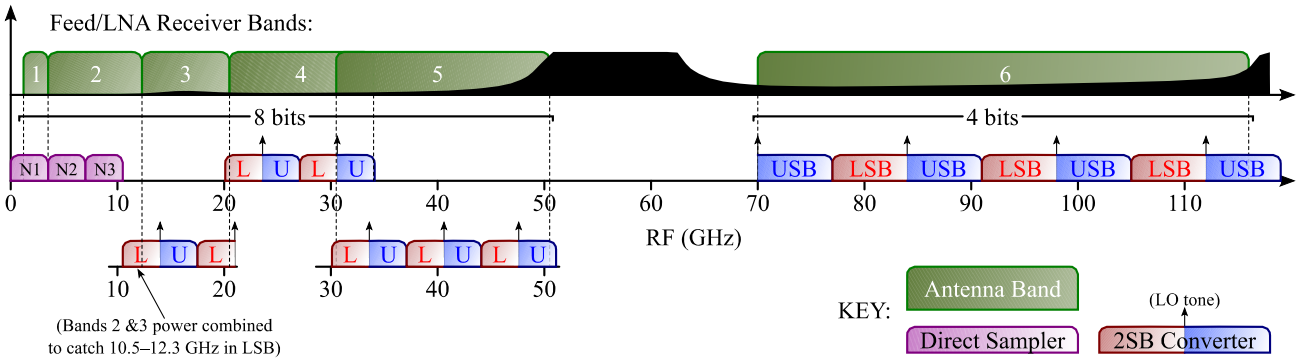


Figure 1 - Block diagram of Integrated Receivers/Downconverters and Digitizers subsystem.

4.2 Subsystem Components

By far, the most significant major components of the IRD subsystem are the receiver modules. As described above, the architecture and frequency distribution of these receiver modules have been designed to cover the required bandwith with the minimum amount of hardware. Figure 2 summarizes the resulting frequency. Note that antennas outfitted with a water vapor radiometer will need an additional two Band 4 modules, included in the table but not shown in the spectrum plot of Figure 2.



Band	Frequency	Receiver Type	# bits	Sample Rate
1	1.2–3.5 GHz	DS	8	7 GS/s
2	3.5–7.0 GHz	DS	8	7 GS/s
	7.0–10.5 GHz	DS	8	7 GS/s
3	10.5–20.5 GHz	2SB	8	7 GS/s
		2SB	8	7 GS/s
4	20.5–34 GHz	2SB	8	7 GS/s
		2SB	8	7 GS/s
WVR (4)	20.5–34 GHz	2SB	8	7 GS/s
		2SB	8	7 GS/s
5	30.5–50.5 GHz	2SB	8	7 GS/s
		2SB	8	7 GS/s
		2SB	8	7 GS/s
6	70–116 GHz	2SB	4	14 GS/s
		2SB	4	14 GS/s
		2SB	4	14 GS/s
		2SB	4	14 GS/s

Figure 2 - Integrated Receiver/Downconverters and Digitizers frequency plan.

4.2.1 Sideband-Separating (2SB) Receiver Modules

A block diagram of a typical 2SB receiver module is shown in Figure 3. Each module has two RF inputs, one for each polarization. These inputs are broadband filtered to limit the power to downstream components, then amplified.

Preferably following the warm RF amplifier is a step attenuator for level control. This ensures that any changes here have minimal effect on the calibration coefficients for sideband-separation. At the highest frequencies, where step-attenuators may not be readily available, this level-control could be moved into the IF signal path. In that case, the M&C software should be programmed to step the attenuators in the I

and Q signal paths synchronously after initial balancing in the lab—again, to ensure minimal impact on the calibration coefficients. Although some uncorrected amplitude imbalance will result from non-uniformity of the step-sizes of the two attenuators, the effect should be sufficiently small that the modules will still easily meet the sideband-rejection specification. All 2SB modules will support a power adjustment range of ±12 dB from nominal. The lower frequency bands may need an additional 30 dB switchable attenuator to support solar observing. This 30 dB of extra attenuation will undoubtedly degrade the noise figure, but this is not a concern for the solar-observing scenario.

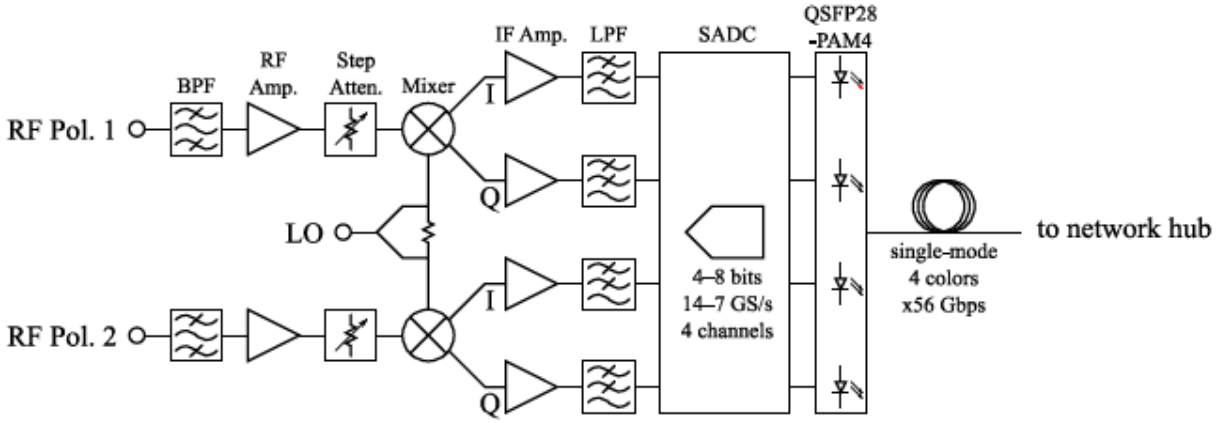


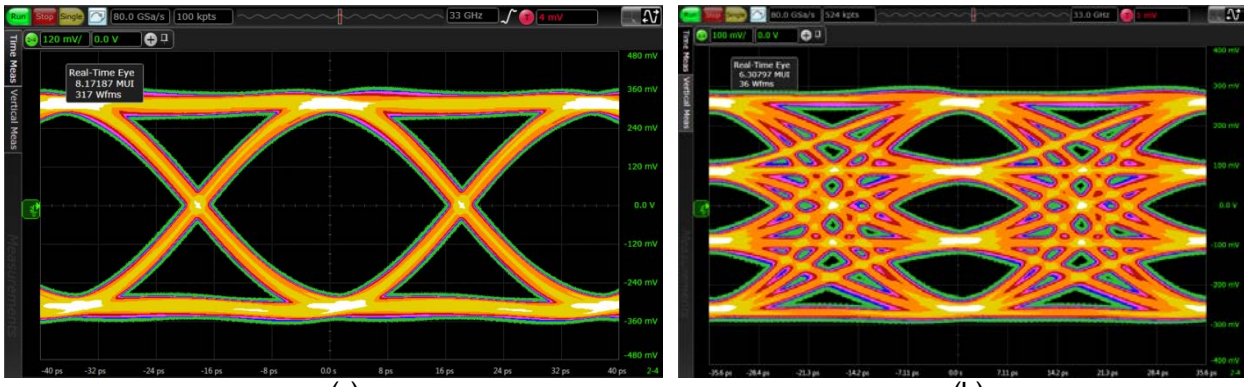
Figure 3 - Block diagram of a sideband-separating (2SB) receiver module.

The mixers implement a single-LO, direct-to-baseband I/Q downconversion. Additional warm-amplification and anti-alias filtering is present at baseband. This is followed by the Serial-ADC (SADC) chip described earlier, either two dual-channel SADCs or a single quad-channel SADC to capture I and Q from both polarizations. The SADC chip is progammable to support multiple bit depths and sample rates. For the highest bands needing the widest bandwidths, we anticipate 4-bit sampling at 14 GS/s. For lower bands, where human interference is more likely an issue, we will use 8-bit sampling at 7 GS/s.

Both sample rates are compatibile with the emerging industry standard serial rate of 56 Gbps per lane. These serial outputs are therefore fed into a quad-channel fiber-optic transceiver capable of transmitting 56 Gbps per lane, where four optical wavelengths are combined onto a single fiber. Although relatively new, such transceivers conforming to the QSFP28 form-factor (shown in Figure 4) are now becoming available with reaches of 500m up to 80 km [RD04–05]. These transceivers modulate the optical carrier at 28 giga-symbols per second using four-level pulse-amplitude modulation (PAM4), thus achieveing the serial rate of 56 Gbps.

Figure 4 - Quad Small Form-Factor Pluggable (QSFP28) optical transceiver.

A comparison of the eye-diagrams for the more common binary NRZ modulation and the PAM4 modulation are shown in Figure 5. The implementations of our unformatted serial link in actual telescope hardware to date have been limited to the NRZ waveform, but calculations show that the PAM4 waveform would be even more robust in our links due to the higher density of transitions for the clock recovery loop to lock onto (see Figure 6).



(a) (b)

Figure 5 - Comparison of (a) binary NRZ and (b) PAM4 optical modulation schemes.

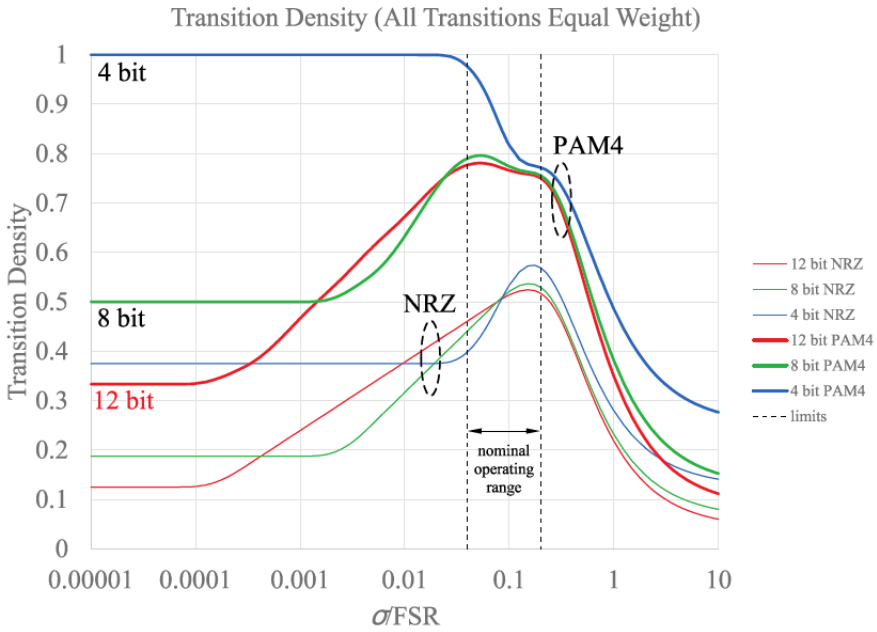
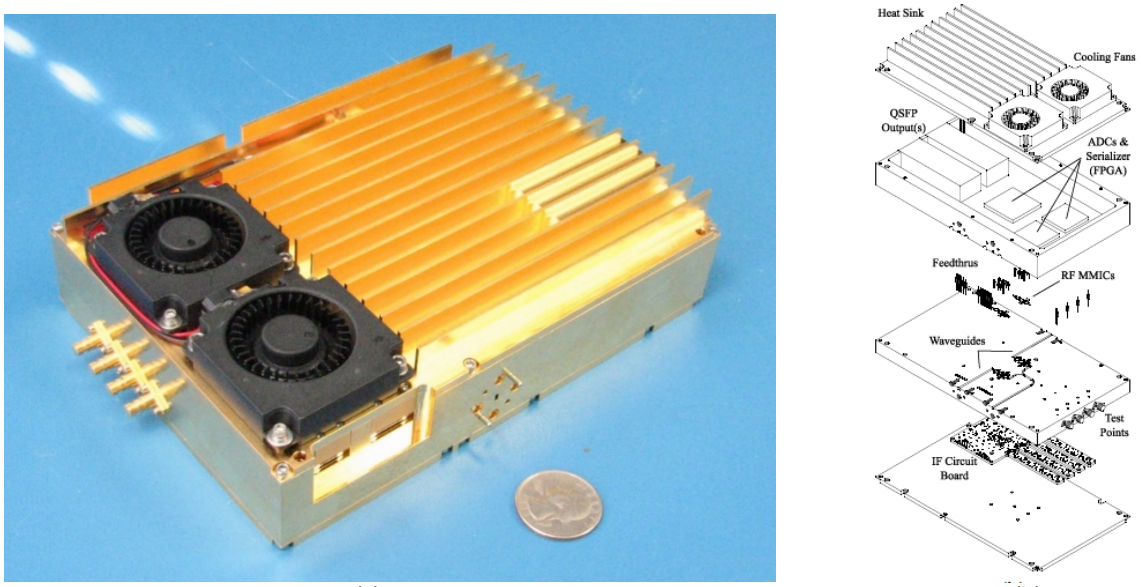


Figure 6 - Transition density for Gaussian-distributed white noise as a function of rms signal amplitude, for both NRZ and PAM4 encoding.

Although the SADC chip which is critical to realizing the SWaP benefits of the proposed design is not yet available, prototyping on fully-functional (but not full-spec) receiver modules has already begun. An example is shown in Figure 7. The internal details of the construction are shown in Figure 7(b).

This dual-polarization module operates in W-band (75–110 GHz) and may be considered an early prototype for the ngVLA Band 6. It utilizes a Kintex7 FPGA to implement the unformatted serialization of the ADC outputs at 8 Gbps. When the SADC chip becomes available, the same function as this FPGA plus the two ADCs will be implemented on a single chip in a 4mm package and consuming 1/25th the

power. This module has two QSFP output connectors (which are really redundant since only one has enough channels to service the whole module).



(a) (b)

Figure 7 - Prototype W-band IRD 2SB receiver module. (a) Photo. (b) Exploded view of internal construction. Note that this is only a prototype. The cooling fans are needed here since the power-saving Serial ADC ASIC was not yet available. The reference design version will be smaller, consume less power, and be cooled without fans by attachment to a temperature-controlled plate.

4.2.2 Direct-Sampled (DS) Receiver Modules

The SADC will have wide analog input bandwidth to support direct-sampling up to the third Nyquist zone for the lower ngVLA bands. A block diagram for such a receiver module is shown in Figure 8. This module begins with a filter or diplexer depending on the RF band (the diplexer is shown), which roughly isolates the individual Nyquist zones for sampling. This is followed by warm amplification, power leveling, additional amplification, and a final anti-aliasing filter before feeding into the SADC chip and QSFP fiber transceiver. From the SADC forward, the data path is the same as it was for the 2SB modules.

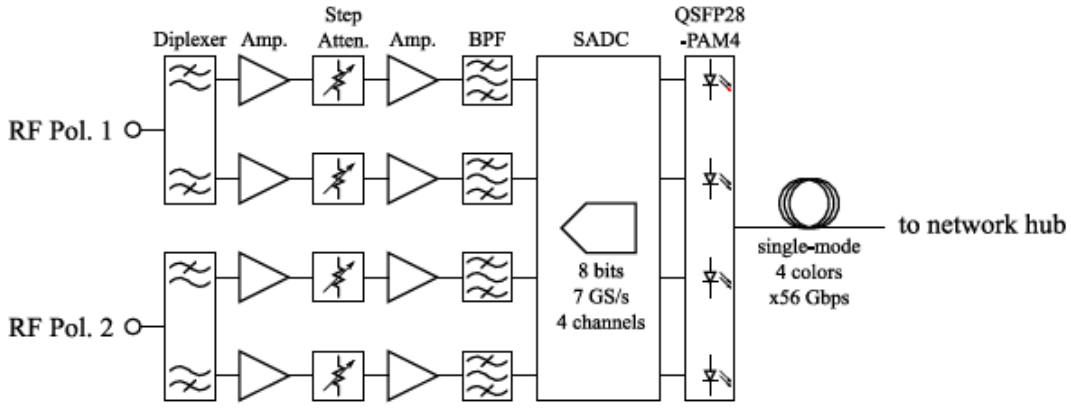


Figure 8 - Block diagram of a direct-sampled (DS) integrated receiver module.

Band 1 will only need two channels (corresponding to the first Nyquist zone for two polarizations) instead of the usual four. Since the commercially available QSFP modules inherently support four duplex, this leaves two lanes unoccupied. The reference design has no predetermined used for these lanes; however, one transmit-receive pair could be configured simply to operate in a loopback mode as part of a round-trip delay measurement in support of the time distribution subsystem, at no extra cost to the IRD modules. Both the 2SB and DS receiver modules are considered line-replaceable units (LRUs) in this design.

4.2.3 Other Components

Other subsystem components include the splitters/combiners that interface these modules to the front-end cryogenics, and the internal interconnects between them and the 2SB/DS receiver modules.

4.3 Interfaces with Other Subsystems

This section provides information about the interfaces of the integrated modules. Interface Control Documents (ICDs) are required between the integrated modules and all connecting systems. In many cases, specifications for the interfaces are not yet available, but the broad scope of the ICD can be defined.

These interfaces shall be developed and documented by the Integrated Receivers and Downconverters designer. Post CoDR, the ICD shall only be updated through formal project change control processes.

Unilateral aspects of the connector interfaces (e.g., M or F) shall refer to the connector on the integrated modules. Cables, waveguide, and fiber runs between the integrated modules and other electronic subsystems are not included in this work package.

4.3.1 Interface to the Cryogenic Front End Subsystem

Signal at Interface	Type	Parameter	Value	Comments
Band 1 RF	Input	Connector Impedance Multiplicity	2.92 mm (F) 50 Ω x2 (one per pol.)	
Band 2 RF	Input	Connector Impedance Multiplicity	2.92 mm (F) 50 Ω x2 (one per pol.)	
Band 3 RF	Input	Connector Impedance Multiplicity	2.92 mm (F) 50 Ω x2 (one per pol.)	
Band 4 RF	Input	Connector Impedance Multiplicity	2.92 mm (F) 50 Ω x2 (one per pol.)	
Band 5 RF	Input	Flange Multiplicity	WR-22 (UG599) x2 (one per pol.)	
Band 6 RF	Input	Flange Multiplicity	WR-10 (UG387) x2 (one per pol.)	

The frequency ranges for these inputs are given in Figure 2. The RF splitters and combiners shown in Figure 1 are included in the IRD subsystem.

4.3.2 Interface to the Water Vapor Radiometer

Signal at Interface	Type	Parameter	Value	Comments
WVR RF	Input	Connector Impedance Multiplicity	2.92 mm (F) 50 Ω x2 (one per pol.)	

4.3.3 Interface to the Timing Reference/LO Subsystem

Signal at Interface	Type	Parameter	Value	Comments
Sample Clock Reference	Input	Frequency Electrical Format Connector Multiplicity	156.25 MHz LVDS TBD x15 (TBC)	Coaxial, shielded
Band 3 LO	Input	Power Level Phase Noise Connector Impedance Multiplicity	>+13 dBm (CW) TBD 2.92 mm (F) 50 Ω x2	
Band 4 LO	Input	Power Level Phase Noise Connector Impedance Multiplicity	>+13 dBm (CW) TBD 2.92 mm (F) 50 Ω x4	
Band 5 LO	Input	Power Level Phase Noise Connector Impedance Multiplicity	>+13 dBm (CW) TBD WR-22 (UG599) 50 Ω x3	
Band 6 LO	Input	Power Level Phase Noise Connector Impedance Multiplicity	>+13 dBm (CW) TBD WR-10 (UG387) 50 Ω x4	

The LO nominal frequencies are given in Figure 1. Each is nominally fixed to simplify calibration and operations, however a ±2 GHz tuning range is supported in order to provide overlap of the adjacent frequency bands so that no frequency "blind spots" exist (except for two narrow slivers between the Nyquist zones of Bands 1 and 2).

4.3.4 Interface to the Monitor and Control Subsystem

Signal at Interface	Type	Parameter	Value	Comments
M&C Serial Bus	Input / Output	Protocol Connector Number of Pins Multiplicity	SPI (mode 0) Nano-D (F) TBD x15 (TBC)	May be combined on the same cable harness with power supplies

4.3.5 Interface to the Power Supplies

Signal at Interface	Type	Parameter	Value	Comments
Analog Positive Supply	Input	Voltage Current Draw Multiplicity	+5 V <1 A (TBC) x15	Internally regulated for multiple voltages.
Digital Positive Supply	Input	Voltage Current Draw Multiplicity	+3.3 V <1 A (TBC) x15	Internally regulated.
Main Negative Supply	Input	Voltage Current Draw Multiplicity	–5 V <100 mA (TBC) x15	Primarily (exclusively?) for transistor gates.

4.3.6 Interface to the Data Transmission Subsystem

Signal at Interface	Type	Parameter	Value	Comments
Digital IFs	Output	Data Format Data Content Connector Physical Format Nominal Wavelength Colors/Lanes Baud Rate Modulation Multiplicity	Unformatted I/Q or Nyquist QSFP Single-Mode Fiber 1310 nm 4 56 Gbps per lane PAM4 x15	PAM4 modulation carries 2 bits per symbol, so "effective" 56 Gbps per lane is achieved by transmitting 28 billion symbols per second.

5 Appendix

5.1 Abbreviations and Acronyms

Acronym	Description
AD	Applicable Document
ADC	Analog-to-Digital Converter
ASIC	Application Specific Integrated Circuit
DBE	Digital Back End
DSP	Digital Signal Processing
DTS	Data Transmission System
IF	Intermediate Frequency
IRD	Integrated Receiver/Downconverter and Digitizer
LO	Local Oscillator
LRU	Line Replaceable Unit
M&C, M/C	Monitor and Control
NES	Near Earth Sensing
ngVLA	Next Generation VLA
NRZ	Non-Return to Zero (binary modulation)
NSF	National Science Foundation
PAM4	Four-level Pulse Amplitude Modulation
PLL	Phase Locked Loop
QSFP28	Quad Small Form-factor Pluggable 28 (giga-symbols per second)
RD	Reference Document
RF	Radio Frequency
SADC	Serial Analog-to-Digital Converter
SerDes	Serializer/Deserializer
SWaP	Size, Weight, and Power
TBD	To Be Determined
VLA	Jansky Very Large Array
WVR	Water Vapor Radiometer

5.2 Bibliography

For more information on the prototypes and techniques employed by the IRD subsystem, the reader is referred to:

M. Morgan and J. Fisher, "Statistical Word Boundary Detection in Serialized Data Streams," U.S. Patent No. 8,688,617, April 1, 2014. People's Republic of China Patent No. 201180046318.8, February 5, 2017.

M. Morgan, S. Wunduke, J. Castro, T. Boyd, and W. Groves, "Compact cm-wave and mm-wave integrated receivers," 32nd URSI General Assembly and Scientific Symposium, Montreal, August 2017.

J. Castro, M. Morgan, J. Ford, and V. van Tonder, "Digital sideband separating downconversion for the Green Bank Telescope phased array feed," URSI National Radio Science Mtg., Boulder, CO, January 2016.

M. Morgan, J. Fisher, and J. Castro, "Unformatted Digital Fiber-Optic Data Transmission for Radio Astronomy Front Ends," *Publications of the Astronomical Society of the Pacific*, vol. 125, no. 928, pp. 695-704, June 2013.

M. Morgan and J. Fisher, "Experiments With Digital Sideband-Separating Downconversion," *Publications of the Astronomical Society of the Pacific*, vol. 122, no. 889, pp. 326-335, March 2010.

M. Morgan and S. Wunduke, "An integrated receiver concept for the ngVLA," *ngVLA Memo #29*, November 2017.

M. Morgan and J. Fisher, "Word-Boundary Detection in a Serialized, Gaussian-Distributed, White-Noise Data Stream," *Electronics Division Technical Note #213*, October 2009.

M. Morgan and J. Fisher, "Simplifying Radio Astronomy Receivers," *NRAO eNews*, vol. 2, no. 3, March 2009

J. Fisher and M. Morgan, "Analysis of a Single-Conversion, Analog/Digital Sideband Separating Mixer Prototype," *Electronics Division Internal Report #320*, June 2008.