Digital Back End/Data Transmission System Reference Design Description

020.30.25.00.00-0002-DSN-A-DBE_DTS_REF_DESIGN

Status: **RELEASED**

PREPARED BY	ORGANIZATION	DATE
J. Jackson, M. Luce, A. Erickson, E. Ford, R. Selina	Electronics Div., NRAO	2018-12-04
S. Durand, Antenna Electronics IPT Lead	Electronics Div., NRAO	2019-04-25

APPROVALS		ORGANIZATION	DATE
R. Selina, Project Engineer	R Selina 2019.07.24 12:10:27 -06'00'	Electronics Div., NRAO	2019-07-24
M. McKinnon, Project Director	Mark McKinnon Digitally signed by Mark McKinnon Date: 2019.07.24 12:38:32 -06'00'	Asst. Director for NM-Operations, NRAO	2019-07-24

RELEASED BY (Name and Signature)		ORGANIZATION	DATE
M. McKinnon, Project Director	Mark McKinnon Digitally signed by Mark McKinnon Date: 2019.07.24 12:38:48 -06'00'	Asst. Director for NM-Operations, NRAO	2019-07-24

Change Record

Version	Date	Author	Affected Section(s)	Reason
0.1	2018-02-12	E. Ford	All	Initial draft, feedback on Sections 3 & 4
1	2018-05-08	J. Jackson	All	First main draft
2	2018-06-04	J. Jackson	All	Many changes
3	2018-07-01	J. Jackson	All	Many changes
4	2018-07-09	J. Jackson	All	Editing, interfaces, fixed change record table
5	2018-08-17	J. Jackson	All	Added text on Sideband Separating Mixer and some general editing
6	2018-09-11	J. Jackson	All	Added SysML diagrams and performed significant final editing
7	2018-09-24	S. Durand	All	Small edits
8	2018-09-27	J. Jackson	All	Reformatting, added SysML structural drawing & text
9	2018-11-06	J. Jackson	5.4 6 Multiple 5.7.2 5.6 3 2.1 5.3 2.2 & 5 5 5 4 & 2.2	Fixed Ethernet specs per RID IPDSR-253 Removed empty section 6 per RID IPDSR-283 Typos fixed per RID IPDSR-156 Text updated per RID IPDSR-282 Text updated per RID IPDSR-280 Added SMF per RIDs IPDSR-272 and 227 RD03 Doc # added per RID IPDSR-139 Updated text per RID IPDSR-275 Updated per RID IPDSR-070 Text updated per RID IPDSR-142 Deleted original Fig 5 per RID IPDSR-155 Defined D501 module per RID IPDSR-276
10	2018-11-15	J. Jackson	Many	General edits
11	2018-11-28	M. Luce A. Erickson	4 & 5	Major edits
12	2018-12-04	J. Jackson	All	General cleanup, added to abbreviations table Rearranged references
13	2019-05-30	R. Selina	All	Minor edits for release; replaced a few figures for readability
A	2019-07-24	A. Lear	All	Incorporated minor edits by M. McKinnon; prepared PDF for signatures and release

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1 Introduction

1.1 Purpose

This document provides a description for the Digital Back End/Data Transmission System (DBE/DTS) subsystem reference design. It covers the design approach, functions, description of key components, interfaces, and risks associated with the reference design. This document will form part of the submission of the ngVLA Reference Design documentation package.

1.2 Scope

The scope of this document covers the entire design of the Digital Back End/Data Transmission System Subsystem, as part of the ngVLA Reference Design. It includes the subsystem's design, how it functions, and its interfaces with the necessary hardware and software systems. It does not include specific technical requirements or budgetary information.

2 Related Documents and Drawings

2.1 Applicable Documents

The following documents may not be directly referenced herein, but provide necessary context or supporting material.

Reference No.	Document Title	Rev/Doc. No.
AD01	Digital Back End and Data Transmission System: Preliminary Requirements	020.30.25.00.00-0001-REQ
AD02	ngVLA Memo 29: An Integrated Receiver Concept for the ngVLA	ngVLA Memo 29
AD04	Antenna Electronics Front End Enclosure Block Diagram	020.30.00.00.00-0002-BLK

2.2 Reference Documents

The following documents are referenced within this text:

Reference No.	Document Title	Rev/Doc. No.
RD01	M. Morgan and J. Fisher, "Statistical Word Boundary Detection in Serialized Data Streams"	U.S. Patent No. 8,688,617, 4/1/2014. People's Republic of China Patent No. 201180046318.8, 2/5/2017.
RD02	M. Morgan, J. Fisher, and J. Castro, "Unformatted Digital Fiber-Optic Data Transmission for Radio Astronomy Front Ends"	*Publications of the Astronomical Society of the Pacific*, vol. 125, no. 928, pp. 695–704, June 2013.
RD03	Integrated Downconverters and Digitizers Design Description	020.30.15.00.00-0002-DSN
RD04	Antenna Electronics Pedestal Enclosure Block Diagram	020.30.00.00.00-0003-BLK

3 Subsystem Overview

The Digital Back End/Data Transmission System receives data from the Integrated Downconverter/ Digitizer subsystem, performs primary digital processing required at the antenna, and prepares data for transmission across private and public telecommunications infrastructure. This subsystem is concentrated in a single, highly integrated RFI shielded module located in the pedestal of each ngVLA antenna.

The module is designated as D501 on the Antenna Electronics Pedestal Enclosure Block Diagram [RD04]. Digital data streams produced in the Integrated Downconverter/Digitizer (IRD) modules located in the Front End (FE) enclosure are received in the D501 DBE/DTS module via 16 single-mode fibers.

Clock recovery and de-serialization is performed on the data, which is then fed to digital processing blocks for functions such as channelization, digital downconversion, re-quantization, and RFI tagging or excision. Finally, processed data is formatted into standard telecommunication formats (e.g., Ethernet, SONET) and returned to the optical domain for transmission over private or commercial fiber optic networks.

Figure 1 and Figure 2 show a SysML block diagram of the Antenna Electronics, highlighting the logical, behavioral, and structural beginnings of the detailed structural design. The network switch block shown is located at the array center ahead of the Central Signal Processing subsystem; the remainder is located at each antenna. The behavioral blocks represent the types of signal processing expected to be performed in the Digital Backend Module FPGA(s).

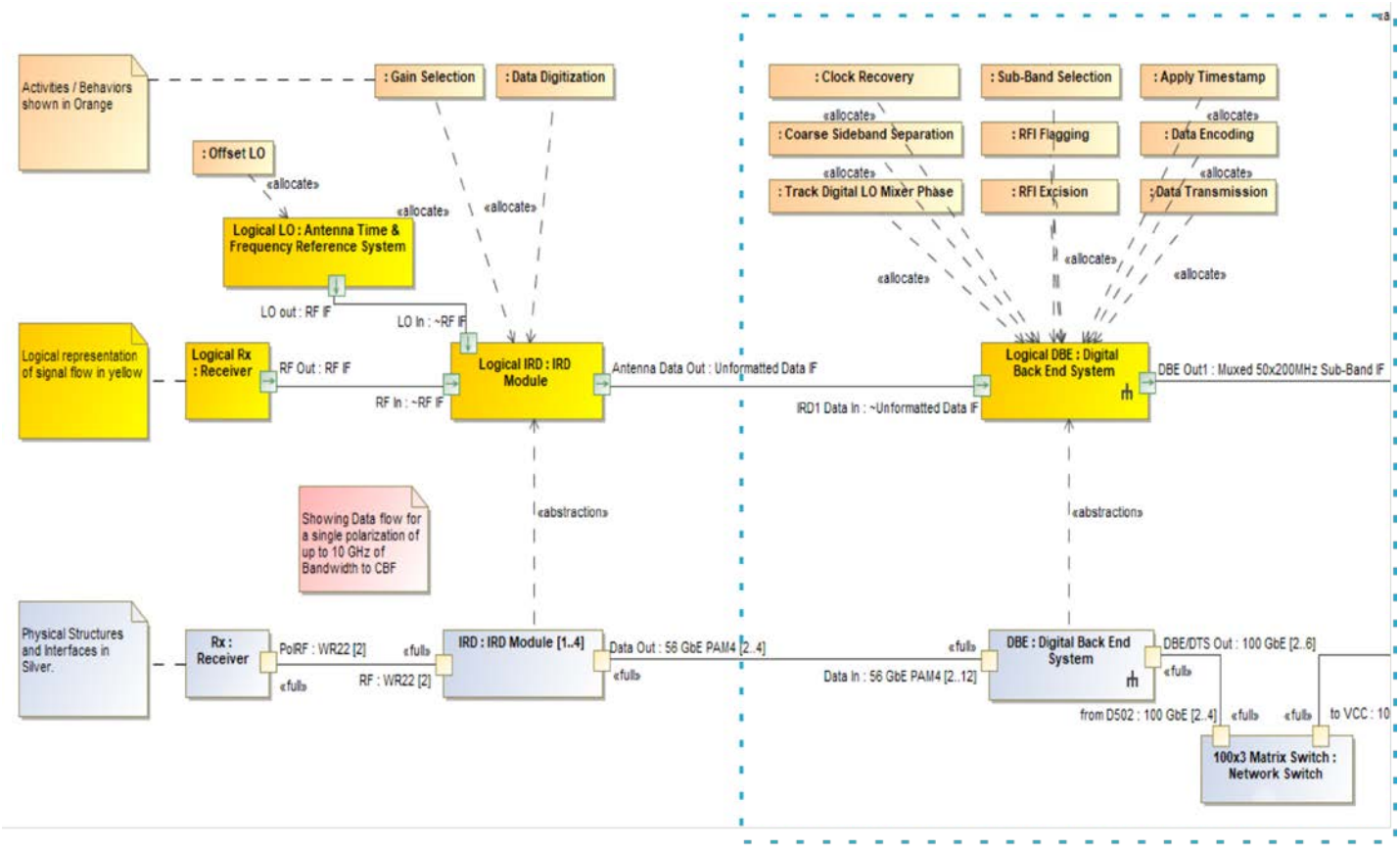

Figure 1 - SysML representation of signal path ahead of the Central Signal Processing subsystem. Behavioral, logical, and structural aspects are shown. Components of the Digital Back End work package are shown in the highlighted block.

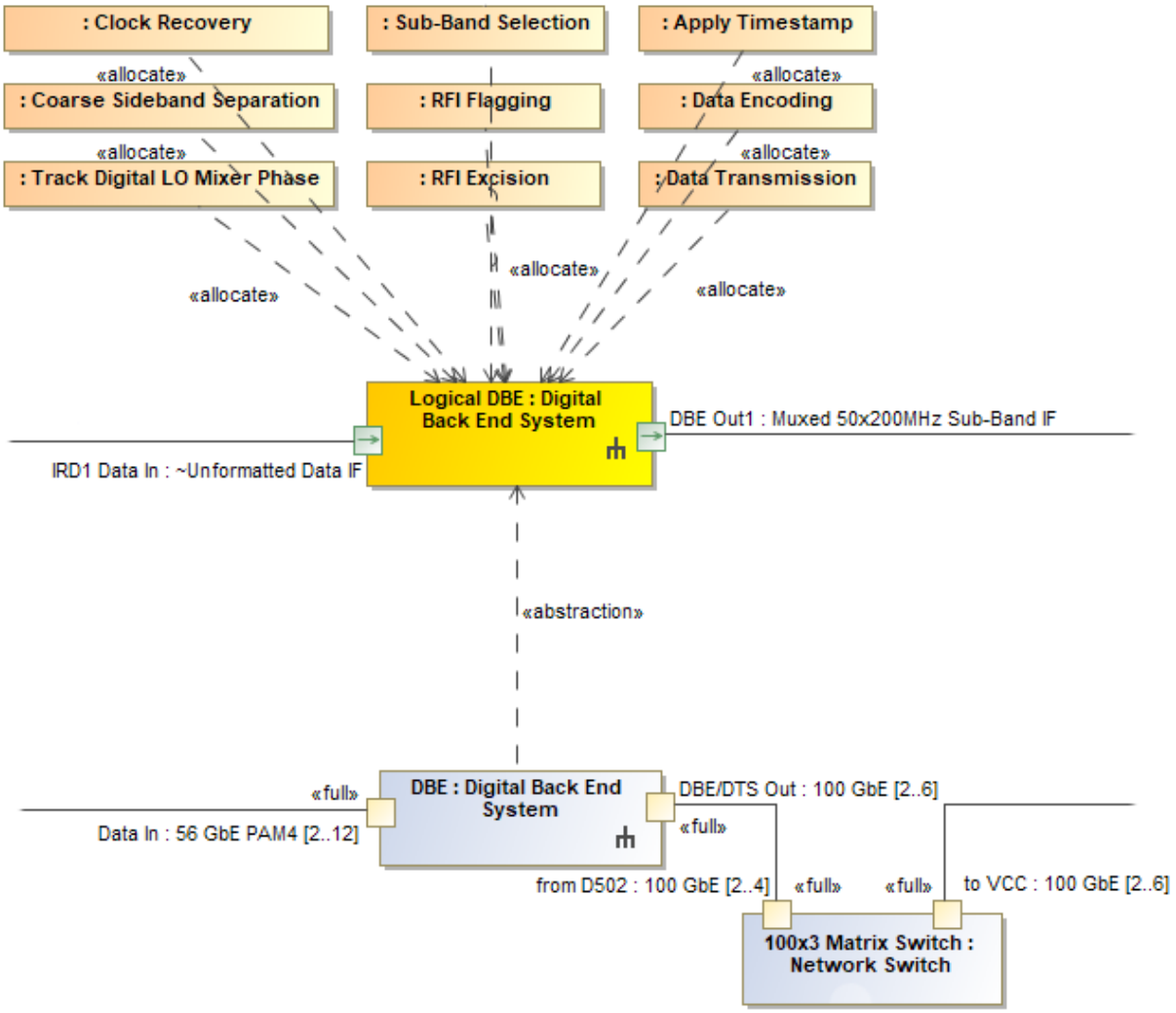

Figure 2 - Close up of SysML representation of DBE subsystem.

4 Subsystem Design

Figure 3 (next page) shows the SysML structural diagram of the Digital Back End (DBE) Module signal path. The optical input modules receive the unformatted optical streams from the IRD modules. All of the digital processing is performed locally in the antenna. Then the data are transmitted to the optical transceivers that interface with the fiber optic cables or to the commercial networking infrastructure that leaves the antenna.

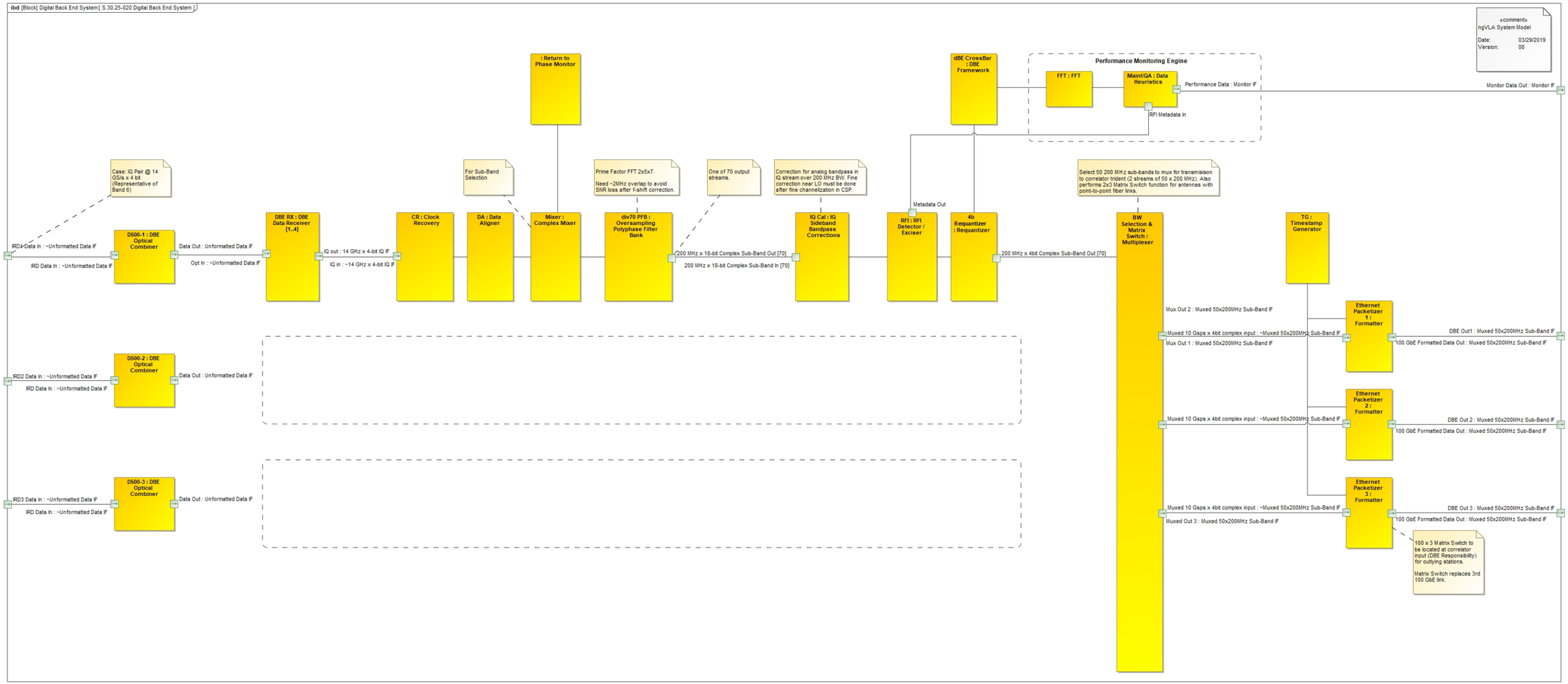

Figure 3 - SysML structural diagram of the Digital Back End module.

The DBE module, itself heavily shielded against RFI, will be further enclosed in a shielded rack in the antenna pedestal. Inside, the optical streams from all IRD modules feed into quad-channel fiber-optic transceivers hosted on printed circuit boards (PCB). The transceivers utilize four wavelengths on a single fiber, one color per lane. They modulate the optical carrier at 28 gigasymbols per second using four-level pulse-amplitude modulation (PAM4), achieving a serial rate of 56 Gbps per lane. These are described in detail in the Integrated Downconverters and Digitizers Reference Design Description (RD03). Physically, the transceivers conform to the QSFP28 form-factor, as shown in Figure 4, and are becoming available with maximum transmission distances between 500 m and 80 km [RD04–05].

Figure 4 - Quad Small Form-Factor Pluggable (QSFP28) optical transceiver.

After conversion to copper (remaining 56 Gbps PAM4) in the fiber transceivers, the IRD data streams will enter one or more large field programmable gate arrays (FPGA) on the PCB via high-speed serializer/deserializer (SERDES) inputs. Once inside the FPGA, the data stream will be processed in multiple ways.

The central digital processing pipeline consists of:

1. SERDES and IRD unformatted link interface,
2. side-band separation,
3. down-conversion, and
4. data encoding and retransmission (SERDES)

A separate processing stream will tap the central data stream for the purposes of RFI excision and flagging. A monitor and control (M&C) processor will also be hosted on a PCB inside the DBE. It will provide all necessary connectivity to the ngVLA monitor/control system. Lastly, the module will include power supplies as necessary for all included hardware.

4.1 IRD Data Stream

The fibers coming from the IRD modules will contain optical carriers of different colors, each carrying 56 Gbps of data. Each pair of those carriers represents raw samples (time-series) from the I and Q outputs of a mixer. At Band 6, these will be 4-bit samples (14 GS/s, or 7 GHz of bandwidth in each I and Q). For simplicity, only one I/Q pair from Band 6 will be transmitted. The data path for each I/Q pair is identical.

4.2 Digital Processing

4.2.1 SERDES

Data from the 44 QSFP28 modules are fed into the high-speed SERDES inputs of FPGAs. These blocks convert the streaming serial data into parallel samples for processing within the FPGA, as Figure 5 shows.

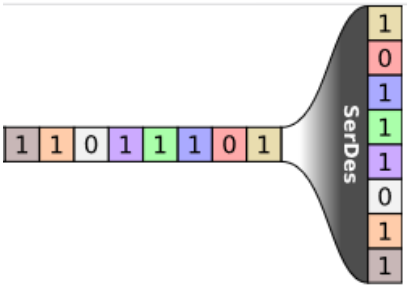

Figure 5 - SERDES functionality.

The current state of the art for production hardware is 58 Gbps/block; technology has been demonstrated for blocks up to 112 Gbps.

4.2.2 Unformatted Link Interface

The IRD subsystem group will deliver a portable FPGA firmware block that acts as a wrapper around the FPGA's built-in Clock and Data Recovery circuitry. This firmware block ensures that the channels are aligned with MSB and LSB in a known, correct state. A monitor/control interface is available to this block for reporting status and receiving commands.

The output from this firmware block will be I and Q time-series samples on parallel pins. To realize a practical design, these streams will be demultiplexed into many more parallel streams at a much slower rate (sequential samples will be clocked out in parallel).

4.2.3 Side-Band Separation

Although sideband separation can be done on time-series data, it is conceptually simpler to do it in the frequency domain. Therefore, the next functional block will be a poly-phase filter bank (PFB) or FFT function. The complex spectra generated in the Fourier transform block accumulate prior to sideband separation. After accumulation, the next functional block separates upper (USB) and lower (LSB) sidebands with a complex mixer (a weighted cross-sum of I and Q spectra), as Figure 6 shows. The weights, or calibration coefficients, are receiver- and frequency-dependent but fairly smooth and can be interpolated.

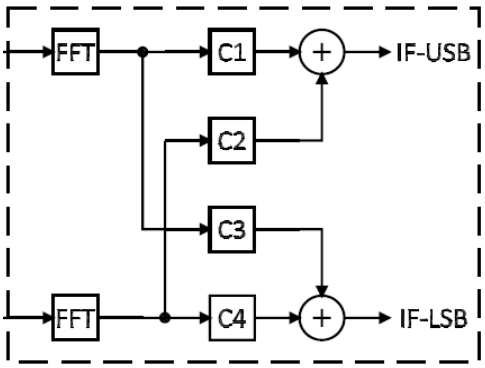

Figure 6 - Side-band separation processor.

4.2.4 Down-Conversion

After side-band select, the data-streams will be down-converted into 50 sub-bands to CSP input specifications (020.40.00.00.00-0001-SPE). Each sub-band will be 200MHz wide and include full bit resolution. This down-conversion will be performed in an over-sampled poly-phase filter bank. This type of PFB provides the desired channelization with a flat pass-band response, and minimizes the spectral image components that are typically found in critically sampled poly-phase filter banks. As Figure 7 shows, the oversampled PFB separates the filter edges in frequency space, reducing the filter overlap which introduces spurious images.

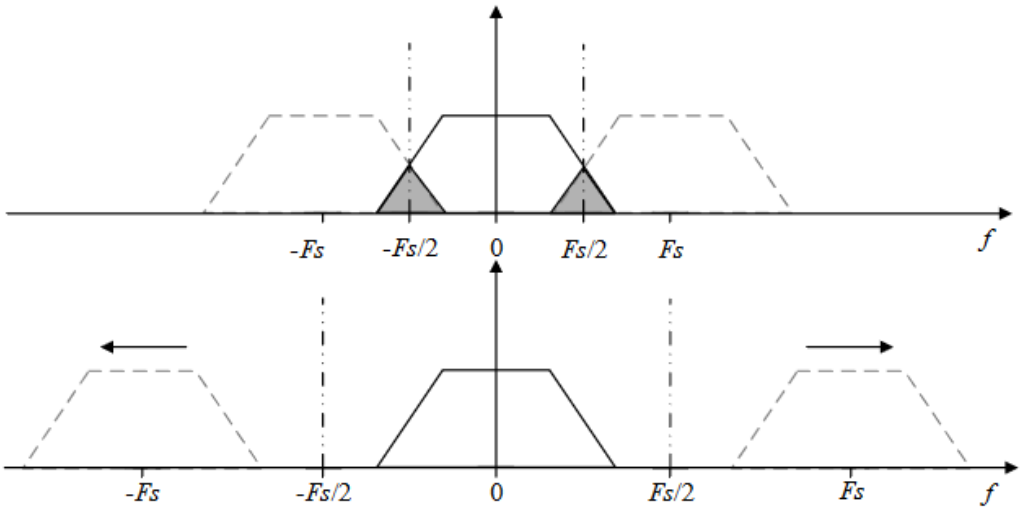

Figure 7 - Critically sampled (M=D) vs. oversampled (M=D×I) PFB.

The most common design approach to these filters simply adds an interpolator (I) after the poly-phase commutator, as shown in Figure 8.

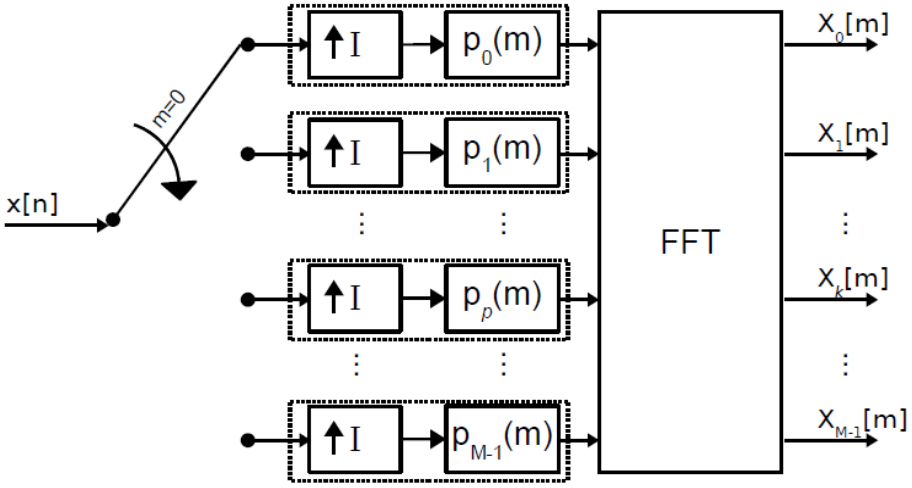

Figure 8 - Oversampled PFB block diagram.

The added interpolator inserts zero padding ($I - 1$ zeros per sample) to the input stream. Otherwise, the poly-phase structure is very similar to the critically sampled case implemented elsewhere in NRAO

systems. This can be implemented in an FPGA using multiple copies of a critically sampled poly-phase filter bank, with some complexity in prototype filter generation.

4.2.5 RFI Excision/Flagging

Digital circuitry inside the FPGA will be reserved for RFI processing. This block will be inserted into the DSP processing pipeline at the appropriate stage. Possible algorithms will be discussed in Section 4.3.

4.2.6 Data Encoding and Retransmission

The last functional block of digital processing will receive data from the down-conversion block and package it for further transmission. This will involve re-quantization, possibly of selectable bit-depth, and packet payload generation. The packets will then flow through an Ethernet IP block and out of the FPGA through another SERDES block (in serializer mode) in standard 802.3 Ethernet format.

4.3 RFI Tagging and Excision

Radio-frequency interference (RFI) will be present in many and changing forms during the lifetime of ngVLA. Cellular networks and satellite downlinks will be the sources of the most prominent signals in correlated data because the same signals will be visible to many antennas, and the signals will be present over an entire integration period. Generally, automatic flagging algorithms can identify these signals in the data at data processing time.

There are also many signals that are expected to affect science data that have high energy but low time occupancy, such as vehicular radar and aviation transponders. These signals are not easily flagged in correlated data, but can negatively affect the science data. Detecting the signals in a high-time-resolution and antenna-specific domain can allow data processing to more intelligently process data to improve science data quality. Firmware in the DBE's signal processing FPGAs will detect these signals using well-known algorithms including spectral kurtosis and spectral peak detection. Flags indicating RFI presence and properties will be transmitted on the Monitor and Control data stream for inclusion into the observation metadata.

4.4 Data Transmission System

Once all local processing and reduction of data is complete, the data streams are fed into the Data Transmission System (DTS) for routing back to the Correlator and Signal Processing system located at the array center. Two configurations shall considered:

The antenna is connected directly to the correlator via NRAO or commercially owned dark fiber.
The data from the antenna is required to be transported through public communications infrastructure.

For antennas in the array core connected directly with dedicated fiber, the data will arrive in sequential order through a single deterministic path. The data will be transmitted using four 100 Gb/s fiber optic Ethernet links using the UDP transport layer protocol. All data will be placed on a single SMF fiber using 100 Gb/s wavelength controlled Ethernet Transceivers on 100 GHz spacing Dense Wavelength Division Multiplexed (DWDM) carriers. Transmission capacity required from each antenna is 400 Gb/s total.

For antennas that cannot be directly connected, the DTS becomes dependent on the telecommunications carrier chosen to service that infrastructure. The network link will be affected by the carrier's local and long haul configuration between the antenna and the array center. NRAO does not have control of the network configuration or the routing of data on the third party carrier's infrastructure. The vendor could either provide dedicated wavelengths on their fibers or require that data be passed through their networks. Data may arrive out of sequence, with unknown transmission delays, error rates and missing

packets. The present design can accommodate a 250 ms delay and tolerates dropped packets. Transmission capacity from the antenna is ideally 400 Gb/s but could be restricted depending on cost and capacity of the commercial carrier and infrastructure local to the antenna.

4.5 Subsystem Block Diagram

Figure 9 shows a block diagram of the hardware structure inside a D501 module. Data stream processing will reside on a high performance PCB. This PCB will contain all of the optical receivers necessary for receiving data from the IRD modules, optical transceivers for the Ethernet links leaving the antenna, and a large FPGA. The FPGA will perform clock recovery, data stream alignment, digital signal processing, and Ethernet framing.

The module will contain a separate PCB to provide all necessary monitor and control. The M&C board will interface to the antenna M&C Ethernet switch via standard SFP modules. It will contain a high performance microprocessor as defined in the M&C subsystem documentation (020.30.45.00.00-0004-DSN). A high-performance microprocessor is necessary in this application because this board will be tasked with acquiring and analyzing multiple data samples for diagnostic and system setup purposes. It will run an embedded variant of the LINUX operating system.

The last PCB in the module will be a high efficiency power supply that converts the antenna's –48 VDC to the voltages for hardware in this module. It will be consistent with the power supply designs described in the DC Power Supply subsystem documentation (020.30.50.00.00-0002-DSN). The power supply PCB will be tailored to provide the unique low-voltage, high-current supply voltages needed by the components in this module.

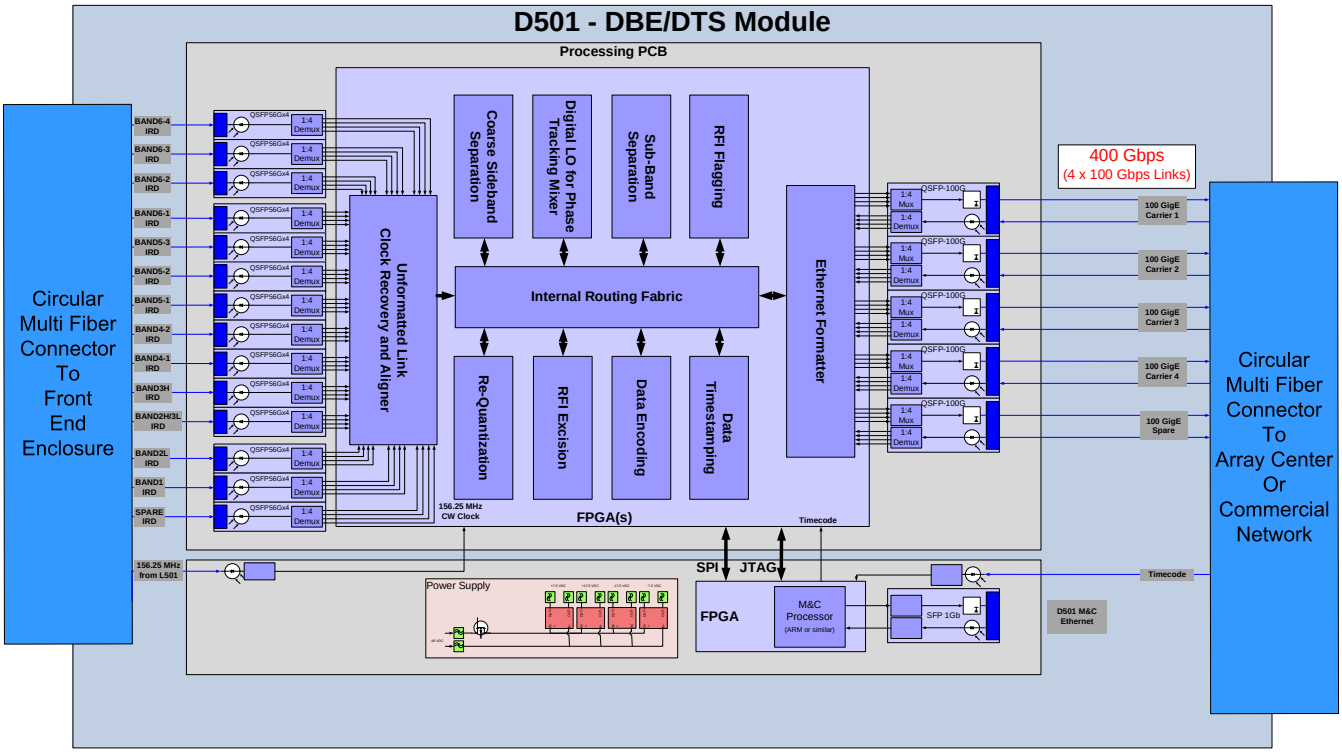

Figure 9 - Block diagram of antenna DBE/DTS subsystem.

4.6 Mechanical Packaging

The D501 DBE Module consists of high-speed digital components, a high-performance microprocessor, and switching power supplies. All of these will contribute to high levels of radio frequency interference that are in-band to the ngVLA, and must be attenuated.

Figure 10 shows a prototype module design based on the Advanced RFI Containment System (ARCS) module system designed for the ngVLA project. This enclosure is heavily shielded to prevent interference with the telescope from the electronics inside. The DBE PCBs will attach to heatsinks inside this module. Two multi-fiber connectors and a filtered Cannon power connector allow signaling and power across the module's RFI shielding.

Module dimensions and aspect ratio are for demonstration purposes and will depend on the space available in the pedestal area enclosure available in the selected antenna design.

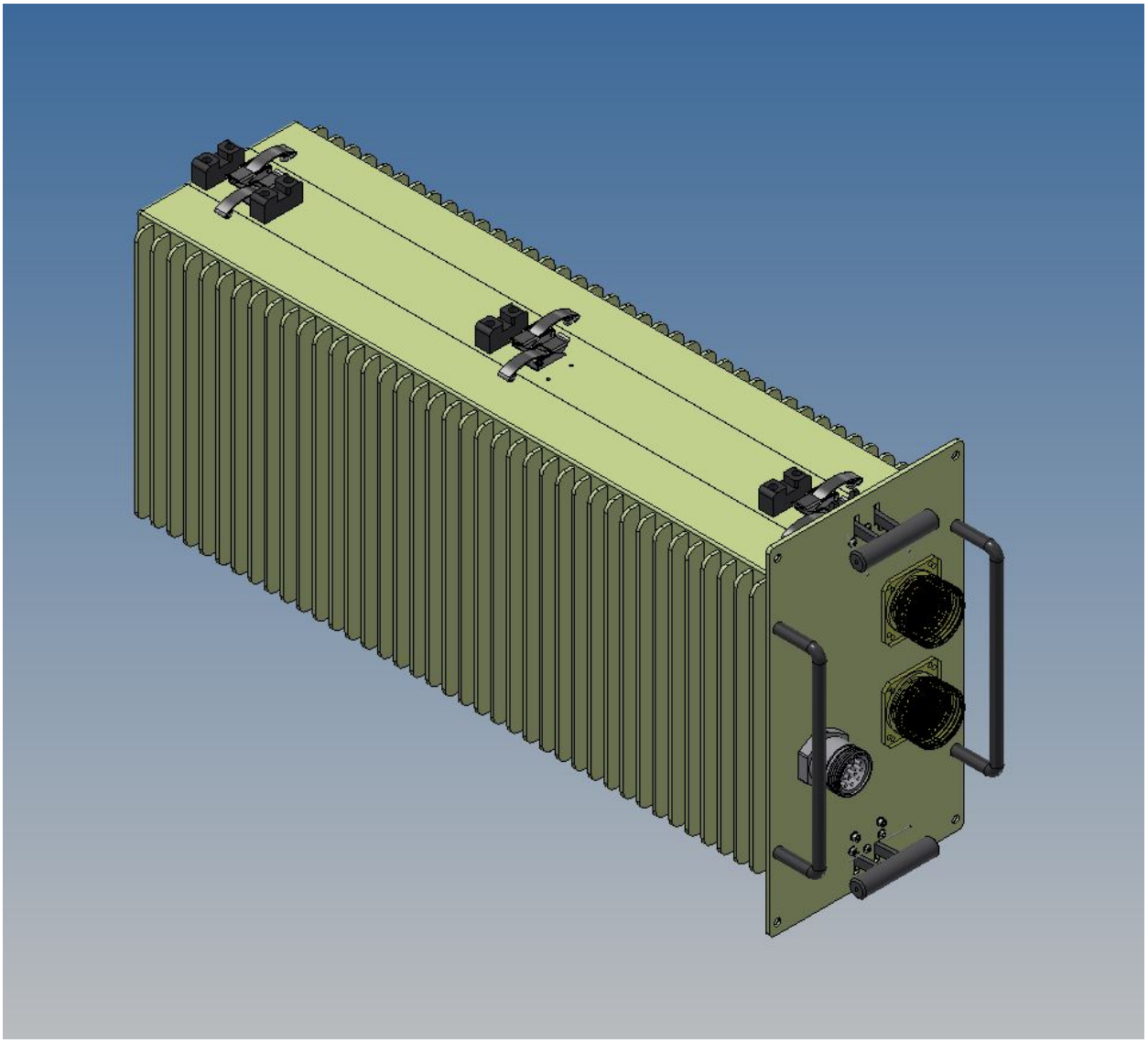

Figure 10 - 3D rendering of D501 module.

4.7 Subsystem Components

4.7.1 High-Level Bill of Materials

- RFI-shielded module metalwork
- Polarization processing PCB (2x), with 2 FPGAs
- Power supply PCB
- Monitor and control PCB
- 16 x 56 Gb/s QSFP modules
- 8 x 40 Gb/s extended range SFP modules
- Power and RF interconnect cable and connectors
- Multi-fiber cables and connectors

4.8 Interfaces with other Subsystems

4.8.1 Power Supply

The D501 will receive –48VDC @10 amps from the power supply subsystem.

4.8.2 LO/Reference

The D501 will require a 156.25 MHz CW tone @0dBm from the LO/Reference subsystem for the generation of internal clocks. The module will also require an optical timecode reference from the LO/Reference subsystem. Specifics of this time code are TBD.

4.8.3 Integrated Downconverter/Digitizer

The D501 will receive data from the Integrated Downconverter/Digitizer modules optically at 56 Gb/s. Power and wavelengths will be determined from specifications of the QSFP fiber transceiver modules chosen for the design.

4.8.4 Data Output

Output data from the D501 will be via standard 100 Gb/s Fiber Optic Ethernet links for antennas connected to NRAO-owned fiber (or located in the central building with the correlator as may be the case for antennas located near the array center). Outlying antennas could be changed to other formats depending on the requirements of commercial fiber infrastructure at each site.

5 Appendix

5.1 Abbreviations and Acronyms

Acronym	Description
AD	Applicable Document
ARCS	Advanced RFI Containment System
CSP	Central Signal Processor Subsystem
DBE	Digital Back End
DSP	Digital Signal Processing
DTS	Data Transmission System
ER-QSFP	Extended Range Quad Small Form-Factor Pluggable Fiber Optic Transceiver
FE	Front End System
FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Array
IF	Intermediate Frequency
IRD	Integrated Downconverter/Digitizer Module
LO	Local Oscillator
LRU	Line Replaceable Unit
LSB	Lower Sideband
M&C, M/C	Monitor and Control
NES	Near Earth Sensing
LSB	Lower Sideband
ngVLA	Next Generation VLA
NSF	National Science Foundation
PFB	Poly Phase Filter Bank
PLL	Phase Locked Loop
QSFP	Quad Small Form-Factor Pluggable Fiber-Optic Transceiver
RD	Reference Document
RF	Radio Frequency
RFI	Radio Frequency Interference
SERDES	High Speed Serial/De-Serializer Input of an FPGA
SMF	Single Mode Fiber
SR-QSFP	Short Range Quad Small Form-Factor Pluggable Fiber-Optic Transceiver
TBD	To Be Determined
VLA	Jansky Very Large Array
WVR	Water Vapor Radiometer