Monitor & Control Hardware Interface Layer: Reference Design Description

020.30.45.00.00-0004-DSN-A-MCHIL_REF_DESIGN

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PREPARED BY	ORGANIZATION	DATE
W. Koski, J. Baca	Electronics Div., NRAO	2019-07-11
S. Durand, Antenna Electronics IPT Lead	Electronics Div., NRAO	2019-07-11

APPROVALS		ORGANIZATION	DATE
R. Selina, Project Engineer	R Selina 2019.07.17 12:36:19 -06'00'	Electronics Division, NRAO	2019-07-17
M. McKinnon, Project Director	Mark McKinnon Digitally signed by Mark McKinnon Date: 2019.07.17 16:37:03 -06'00'	Asst. Director, NM-Ops, NRAO	2019-07-17

RELEASED BY (Name and Signature)		ORGANIZATION	DATE
M. McKinnon, Project Director	Mark McKinnon Digitally signed by Mark McKinnon Date: 2019.07.17 16:37:18 -06'00'	Asst. Director, NM-Ops, NRAO	2017-07-17

Change Record

Version	Date	Author	Affected Section(s)	Reason
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07	2018-10-24	W. Koski	All	James Robnett's RID input
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A	2019-07-17	A. Lear	All	Prepared PDF for approvals & release

Table of Contents

1 Introduction

1.1 Purpose

This document provides a description for the Monitor and Control Hardware Interface Layer (M&C HIL) subsystem reference design. It covers the design approach, functions, description of key components, interfaces, and risks associated with the reference design. This document will form part of the submission of the ngVLA Reference Design documentation package.

1.2 Scope

The scope of this document covers the entire design of the M&C HIL subsystem as part of the ngVLA Reference Design. It includes the subsystem's design, how it functions, and interfaces with the necessary hardware and software systems. It does not include specific technical requirements or budgetary information.

This document is to define the design description for the M&C at the hardware layer or level. This document will define the ngVLA project deliverable as an in-house designed Module Interface Board (MIB), similar to the EVLA project MIB. Because the system touches upon or is part of all equipment in the antenna, possible sub-buildings, and the main central control building, there must be a high level of collaboration between all other Integrated Product Teams (IPT) as their requirements will influence the M&C requirements and vice-versa.

In the Appendix, Figure 3 depicts the EVLA MIB and Figure 4 depicts the companion analog to digital board as visual examples.

2 Related Documents and Drawings

2.1 Applicable Documents

The following documents may not be directly referenced herein but provide necessary context or supporting material.

Reference No.	Document Title	Rev/Doc. No.
AD01	ngVLA Science Requirements	020.10.15.00.00-0001-REQ
AD02	ngVLA System Requirements	020.10.15.10.00-0003-REQ
AD03	System-Level Architecture Model	020.10.20.00.00-0002-DWG
AD04	Environmental Specification	020.10.15.10.00-0001-SPE
AD05	System EMC and RFI Mitigation Requirements	020.10.15.10.00-0002-REQ

2.2 Reference Documents

The following documents are referenced within this text:

Reference No.	Document Title	Rev/Doc. No.
RD01	Antenna Electronics Front End Enclosure Block Diagram	020.30.00.00.00-0002-BLK
RD02	Antenna Electronics Pedestal Enclosure Block Diagram	020.30.00.00.00-0003-BLK

3 Overview: Monitor and Control Devices by Location

The term *device* represents a physical device such as a LRU or other hardware unit that is to be monitored and controlled. A *MIB device* has an internal MIB providing all M&C functions taking place within the device. A *satellite device* type has interface circuitry to which an external MIB device communicates. A *high-level device* has higher requirements, especially for storage and computational power.

An example of a MIB device is the L502 whose MIB is connected to an analog board and a FPGA inside the device. Some examples of satellite devices are the T501 through T513, which linked to the F523 MIB device via serial communications. An example of a high-level device is the M500 Supervisor, which has higher storage and computational capacity necessary to carry out its functions.

3.1 Subsystem Block Diagram

Figure 1 and Figure 2 show the Monitor and Control Subsystem block diagrams for the interface protocol identification and the routing scheme plan.

Two antenna locations contain equipment requiring MIB devices: the Front End Enclosure and the Pedestal Enclosure. Table 1 lists all devices at the Front End location, and ngVLA Document #020.30.00.00.00-0002-BLK [RD01] presents a block diagram of the Front End Enclosure. Table 2 lists all devices at the Pedestal location, and ngVLA Document #020.30.00.00.00-0003-BLK [RD02] presents a block diagram of the Pedestal Enclosure.

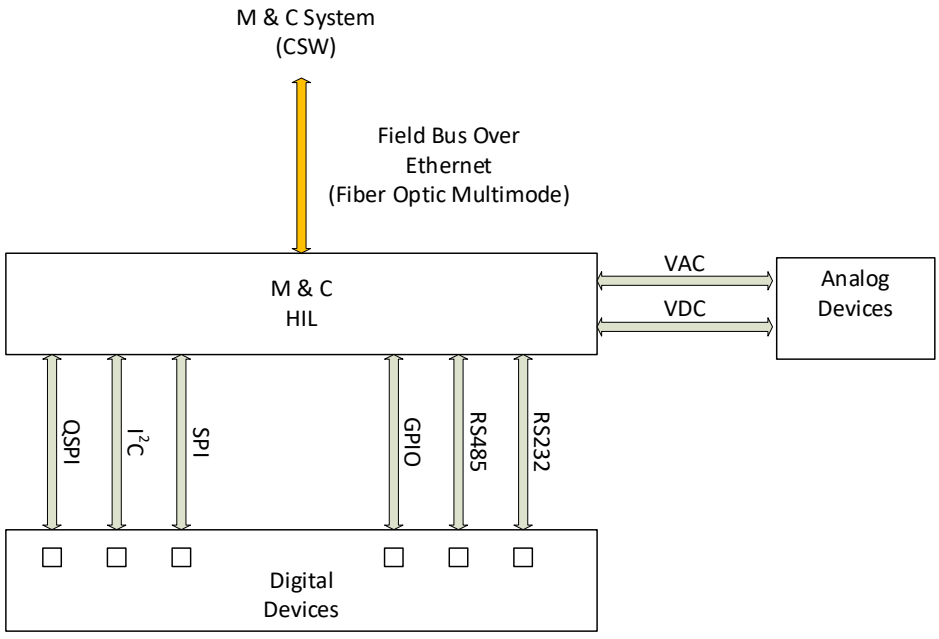

Figure 1 - Monitor & Control system interface protocol plan. The M&C HIL interfaces to analog and digital devices over a wide variety of protocols, while providing a single field bus over Ethernet interface to the M&C software system.

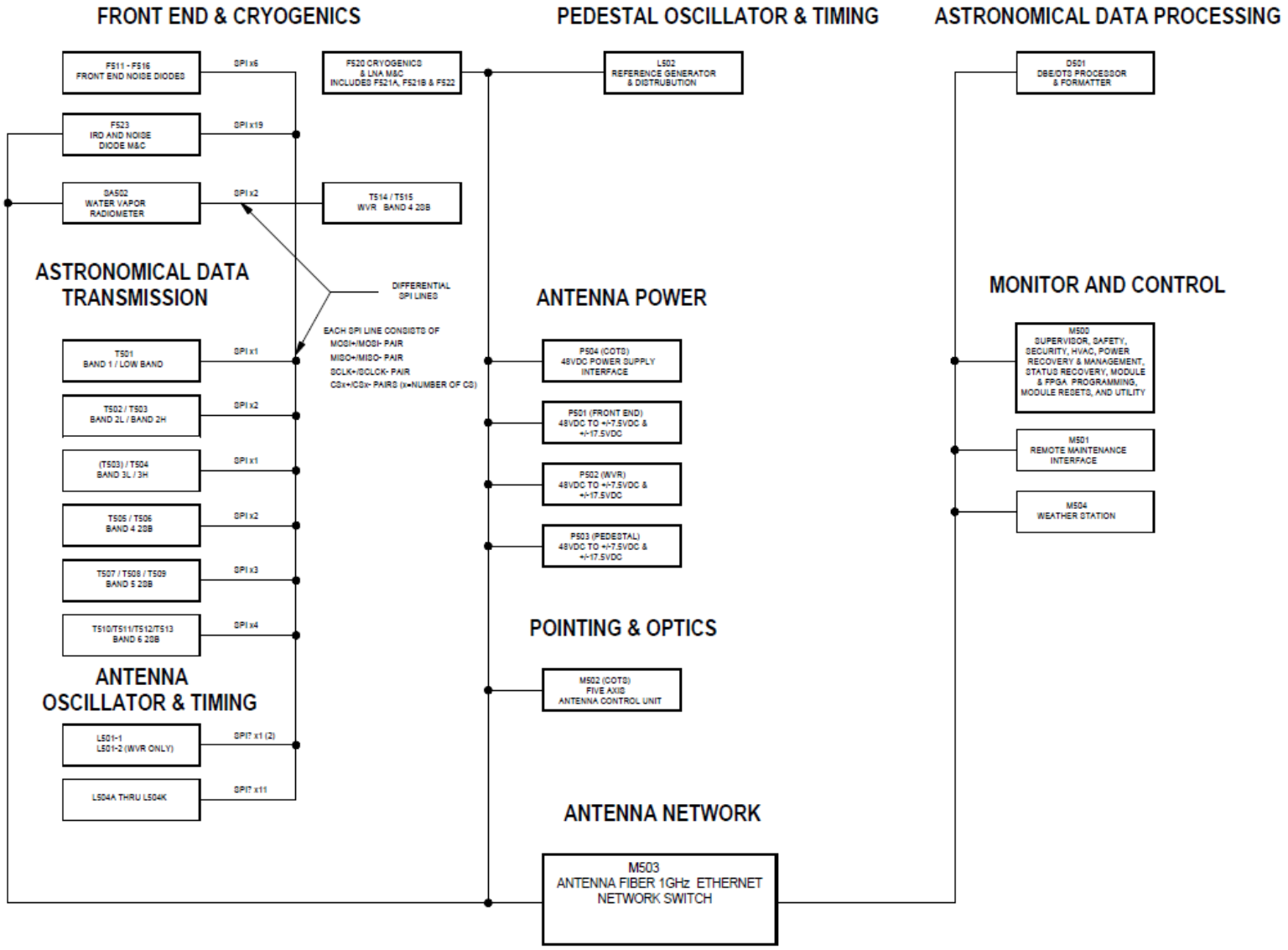

Figure 2 - Monitor & Control system routing scheme diagram for ngVLA reference array at the hardware layer. ngVLA Document #020.30.45.00.00-0001-BLK shows the diagram at full size.

3.2 Antenna Front End Enclosure Device Possibilities

Device	Description	Type	Quantity	Notes
F511–F516	Noise Diode	Satellite	6 (SPI)	F523 Satellites
F520	Cryo and LNA M&C	High-Level	1	Satellites out to F521A, F521B, & F522
F521A	Dewar A Cryogenics Driver	Satellite	1	F520 Satellite
F521B	Dewar B Cryogenics Driver	Satellite	1	F520 Satellite
F522	Vacuum Pump Driver	Satellite	1	F520 Satellite
F523	IRD & Noise Diode M&C	MIB	1	Satellites out to F511–F516, L501-1, (L501-2), L504 & T501–T513
L501-1, L501-2	LO Reference & Sample Clock Generator	Satellite	1 (2)	F523 Satellite (L501-2) Only for WVR Antennas
L504-A–K	LO Generators	Satellite	11	F523 Satellite
T501, T502	BAND 1 IRD Device BAND 2 IRD Device	Satellite	2 (SPI)	F523 Satellites
T503	BAND 2/3 IRD Device	Satellite	1 (SPI)	F523 Satellite
T504	BAND 3 IRD Device	Satellite	1 (SPI)	F523 Satellite
T505, T506	BAND 4 IRD Device BAND 4 IRD Device	Satellite	2 (SPI)	F523 Satellites
T507–T509	BAND 5 IRD Device	Satellite	3 (SPI)	F523 Satellites
T510–T513	BAND 6 IRD Device	Satellite	4 (SPI)	F523 Satellites
SA502	Water Vapor Radiometer	MIB	1	Only for WVR Antennas
T514, T515	WVR BAND 4 IRD Device	Satellite	2 (SPI)	Only for WVR Antennas SA502 Satellites
P501	Power Supply	MIB	1	
P502	Power Supply	MIB	1	Only for WVR Antennas

Table 1 - Front End enclosure M&C device list.

3.2.1 Front End Interface Devices

The F520 has a high-level MIB and is responsible for biasing the low noise amplifiers for Bands 1–6. It also has the cryogenic system control for satellite LRUs: Dewar A Cryogenics Driver (F521A), Dewar B Cryogenics Driver (F521B), and Vacuum Pump Driver (F522).

The F523 IRD & Noise Diode M&C LRU monitors and controls IRD LRUs (T501–T513) and Noise Diode LRUs (F511–F516) for Bands 1–6 via 19 SPI interfaces. The L501 (-1,-2) LO Reference & Sample Clock Generators and L504 (-A–K) LO Generators are satellites as well, but their 12 to 13 interfaces have not been established (they will likely be SPI).

The SA502 is similar to the F523 but is only on selected antennas that have the water vapor radiometer (WVR) installed. It contains two SPI interfaces for the IRD LRUs T514 and T515. Its temperature control subsystem keeps IRD LRUs T514 and T515 at a controlled, stable temperature. Note that for the final design there may be a WVR for each antenna, this drives only needing the F523.

3.2.2 Local Oscillator Devices

The L501-1 and L501-2 (only if WVR is installed) are LO Reference and Sample Clock Generators. The L504 (-A–K) LO Generators are satellite LRUs to the F523 LRU.

3.2.3 IRD Devices

The T501 through T513 LRUs and the optional WVR T514 & T515 LRUs sample RF astronomical information at high speed and convert it to the digital stream sent on fiber to the D500. On each T5XX device is a serial peripheral interface (SPI) connected to the F523 or the SA502 on copper differential signal lines. Normally SPI consists of master out/slave in (MOSI), master in/slave out (MISO), serial clock (SCLK), and either none, one, or multiple low true chip select (CS*) lines. For the T501 through T513 alone, this would mean 78 (none), 104 (one), or 208 (multiple assuming five CS* lines) copper connections.

3.2.4 Power Supply Devices

The P501 and P502 power supply devices have a MIB and analog board.

3.3 Pedestal Enclosure Device Possibilities

Device	Description	Type	Quantity	Notes
D501	DBE/DTS Device	High-Level	1	
L503	Reference Receiver, Generator, & Distribution Device	MIB	1	
M500	Supervisor Device	High-Level	1	Single point of failure
M501	Maintenance Device	High-Level	1	M500 redundancy?
M502	Five Axis Control Device	High-Level	1	COTS device? MIB added
M503	Ethernet Fiber Switch	High-Level	TBD	COTS device; M&C included
M504	Weather Station Device	MIB	1	For weather station antennas only. Satellites to instruments via RS232
M505	Utility LRU	MIB	1	–48VDC power supply, HVAC, etc.
P503	Pedestal Power Supply	MIB	1	
P504	48VDC Power Supply	MIB	1	COTS device; M&C included

Table 2 - Pedestal Enclosure M&C device list.

3.3.1 DBE/DTS Devices

The D501 DBE/DTS LRU uses a high-level MIB that will monitor and control the Polarization A and B processing devices for astronomical data needs. These include clock recovery & aligner, channelization, RFI, quantization, future digital, internal routing fabric, and Ethernet formatter. The high-level MIB connects to its own FPGA, which in turns provides SPI and JTAG connections for each polarization device. It must store all functional data routing, processing codes, and formats for the various data transmission methodologies.

3.3.2 Local Oscillator Devices

The L503 Reference Receiver & Generator and Distribution LRU has a MIB and analog board that includes a FPGA interface for its functionality.

3.3.3 Monitor and Control Devices

The M500 Supervisor LRU has a high-level MIB and this device has the following functional capabilities beyond the Supervisor role: safety, security, HVAC, power recovery and management, and status recovery. The M500 presents a single-point-of-failure risk, so redundant functionality is desirable.

The M501 Remote Maintenance Interface LRU has a high-level MIB and is a candidate for M500 redundancy, provided the redundancy requirement requires separation. With 263 ngVLA antennas proposed, remote

maintenance will be essential to determine issues that affect the array's ability to carry out scientific observations. It may be part of the M&C system as in the original VLA design, with two monitor streams: one used by the operating system, the other devoted to maintenance and under technical staff control. This device would stream complex information to remote users monitoring a situation via oscilloscope, spectrum analyzer, logic analyzer, and signal generator. It could also include visual and aural capabilities to determine unusual sounds and, upon detection, activate a robotic camera (or even a drone) to examine the antenna and transmit information for maintenance, safety, and security.

The M502 Four-Axis Antenna Control Unit (ACU) and focus translation mount (FTM) device has a high-level MIB interface. As this is considered a COTS device provided by the antenna manufacturer, NRAO may have to contractually make the high-level MIB chosen by NRAO identical to the one in this device, otherwise this MIB will be unique.

The M503 Ethernet Switch device is COTS and has a high-level MIB with a unique design. It currently specifies 32 fiber connections to the Ethernet switch at 1 GHz. However, the connections do not account for local maintenance ports for laptops, test equipment, LabVIEW, etc., so 40–48 is a reasonable range for Ethernet switch port connections.

The M504 Weather Station device uses a MIB or high-level MIB to monitor weather conditions at the antenna, especially for remote antennas located distantly from the core. Not every antenna would necessarily have a weather station; rather, antennas would be chosen that could manage an array cluster group. The station sensors would measure temperature, dew point, and barometer, mounted on the dish backside to be level with or higher than the feeds as the antenna tracks, or on a fold-over tower. On the tower would be wind speed and wind direction, making it very light as these instruments add little weight.

The M505 Utility uses a MIB analog board that would monitor Antenna environment and provide environmental controls.

3.3.4 Power Supply Devices

The P503 Power Supply device uses a MIB and analog board.

The P504 has a MIB and analog board to monitor and control the –48V DC power supply subsystem. This COTS device may have a built-in M&C interface, which like the M503 would be unique.

3.4 Interfaces with Other Subsystems

The M&C HIL stands between the network and the subsystem devices. Therefore, the ICD for the network side uses standard Ethernet protocols such as TCP/IP, UDP, ICMP, RDP, 3PC, etc. However, the Ethernet standards do not preclude NRAO from devising their own in-house protocols.

For the sub-system devices, the MIB will provide interfaces such as PC104, 3-Wire SPI, 4-Wire SPI, QSPI, I^2C, GPIO, RS232, RS485, etc. Once the interfaces for the MIB have been determined, the ICD would indicate what is available, while the sub-system ICD will determine interface choice(s) and how it will use them. This includes deviations from best practices and any specialized protocols for message or data transmissions.

4 Appendix

4.1 Monitor and Control Amounts and Cost

The 15-year budget for the M&C HIL (020.30.15.00.00-0003-BUD) bases total cost for the MIB and analog boards on the known NRE and production costs during the EVLA project, adjusted for inflation. The digital card cost was based on the current cost for a similar card that was developed for the EVLA WVR project.

The cost of satellite cards, which may not fall under the purview of M&C, is an estimation. The high-level MIB cost is based upon the Advantech PCM-3365EW-S9A1E, a commercial PC104 board having maximum solid state storage and additional memory added.

LRU costs are based on recent quotations for metalwork machining, combined with the high-level MIB cost above, except for the M504 which assumes usage of the standard MIB combined with a lower quantity requirement of 55 M504s.

4.2 Interface Boards

EVLA designs requiring M&C have a main board with an area for the connectors and mounting holes needed to place the analog board and/or the module interface board (Figure 3) upon it. This provides an adaptable system such that if no analog board is needed, the designer installs only the MIB. If needed, the analog board (Figure 4) is installed onto the main board first, then the MIB is placed on the analog board.

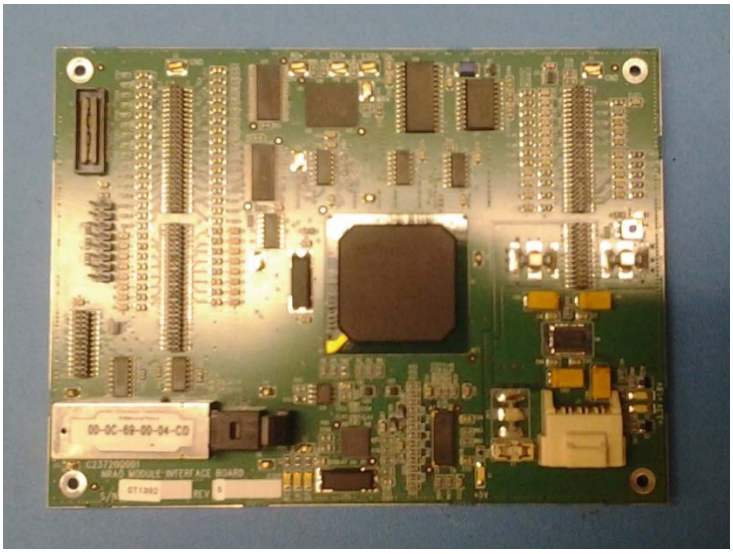

Figure 3 - EVLA module interface board.

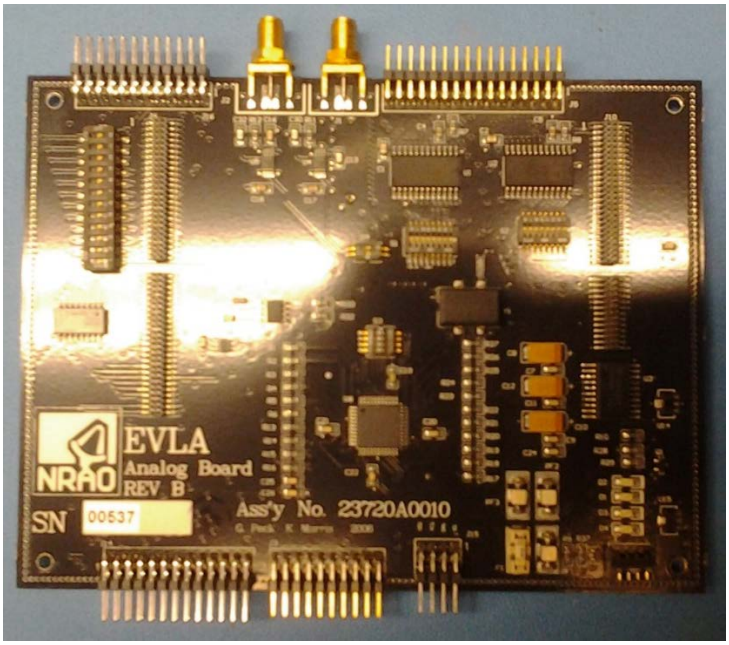

Figure 4 - EVLA analog board.

4.3 Abbreviations and Acronyms

Acronym	Description
AD	Applicable Document
DBE	Digital Back End
DTS	Data Transmission System
IF	Intermediate Frequency
LO	Local Oscillator
LRU	Line Replaceable Unit
M&C, M/C	Monitor and Control
M&C HIL	Monitor and Control Hardware Interface Layer
MIB	Monitor & Control Interface Board
NES	Near Earth Sensing
ngVLA	Next Generation VLA
NSF	National Science Foundation
PLL	Phase Locked Loop
RD	Reference Document
RF	Radio Frequency
TBD	To Be Determined
VLA	Karl G. Jansky Very Large Array
WVR	Water Vapor Radiometer