Integrated Downconverters and Digitizers

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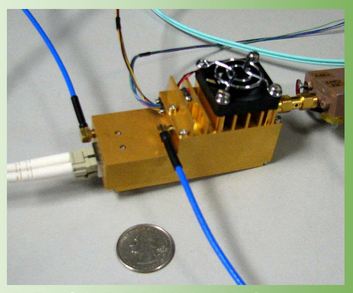
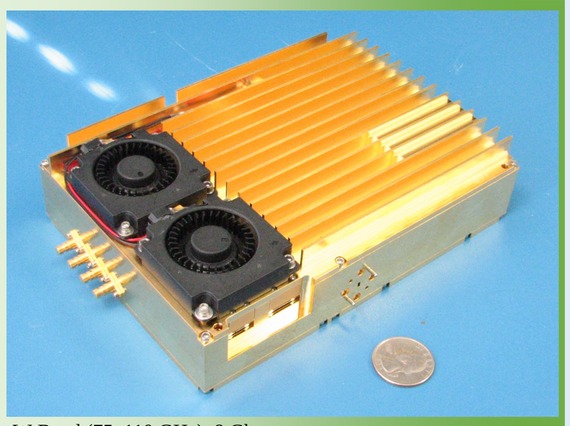
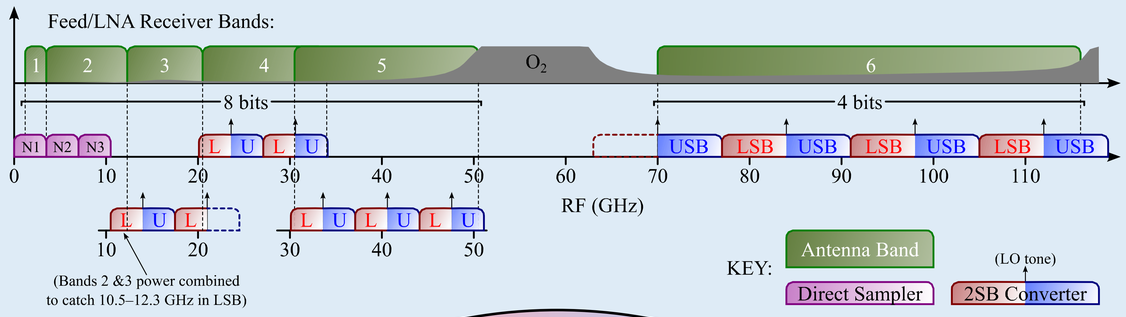
Early Prototypes



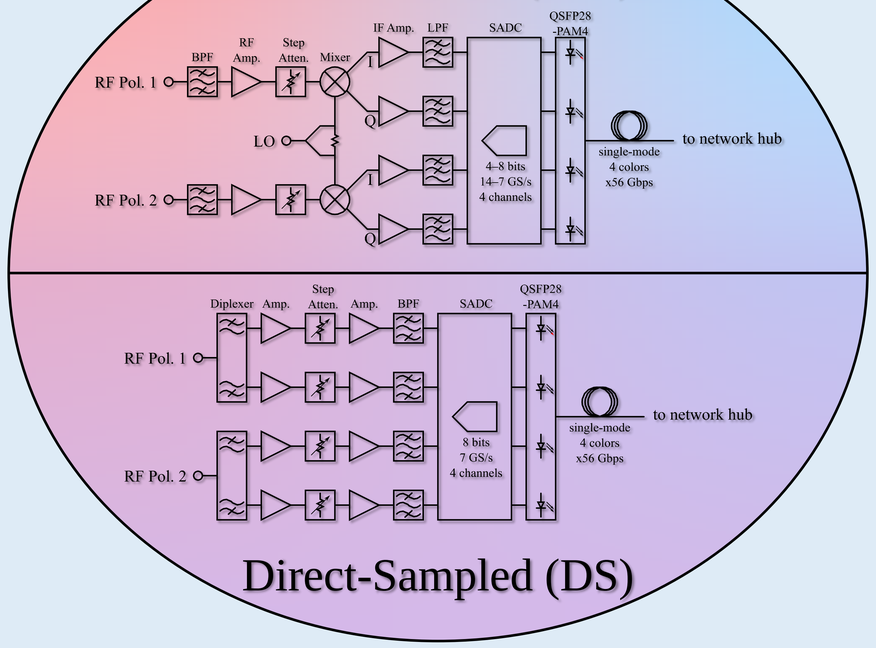
L-Band (1.7–2.6 GHz), 2.5 Gbps output



W-Band (75–110 GHz), 8 Gbps output

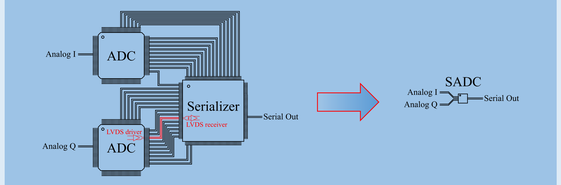


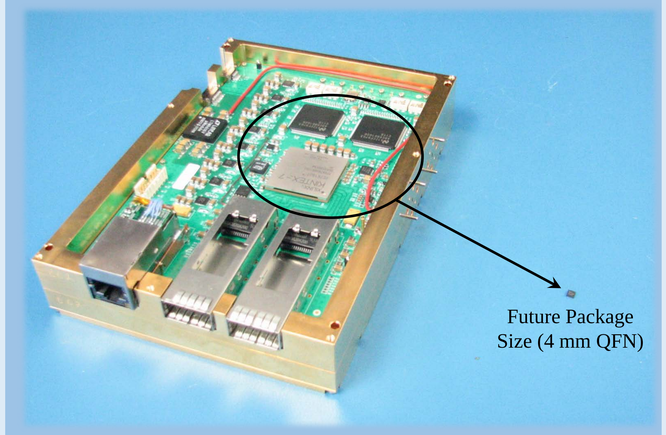
Two-Sideband (2SB)



Serial ADC (SADC)

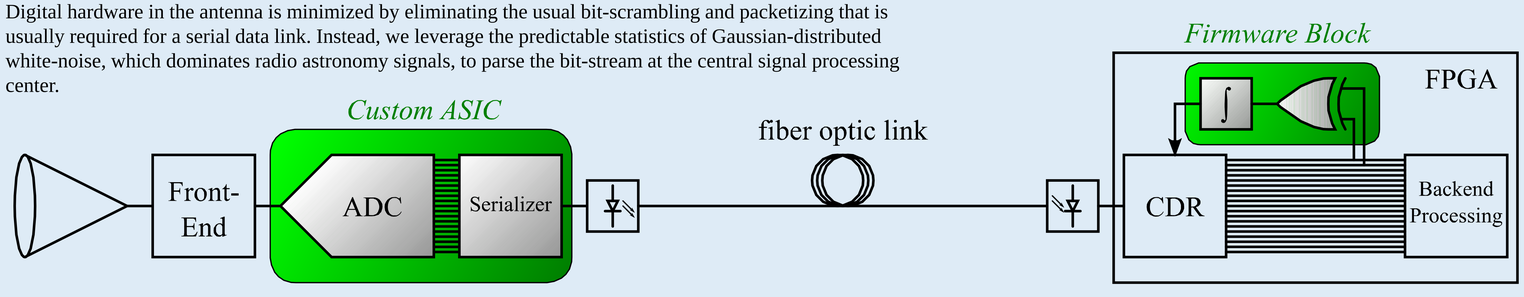
By integrating the ADC and Serializer on a single ASIC, we achieve a orders of magnitude reduction in footprint and power dissipation for these functions.





Unformatted Serial Data Transfer:

Digital hardware in the antenna is minimized by eliminating the usual bit-scrambling and packetizing that is usually required for a serial data link. Instead, we leverage the predictable statistics of Gaussian-distributed white-noise, which dominates radio astronomy signals, to parse the bit-stream at the central signal processing center.



First Article Prototype
(under development)

- Serial rate = 10 Gbps
- Resolution (dynamic) = 2–8 bits
- Sample rate:
  - 5 GS/s @ 2 bits
  - 2.5 GS/s @ 4 bits
  - 1.25 GS/s @ 8 bits
- Analog Input BW = 7.5 GHz
- Power dissipation = **225 mW!**
- Footprint:
  - ~2 mm die
  - 4 mm QFN package

Future Upgrade
(ngVLA reference design)

- Serial rate = 56 Gbps
- Resolution (dynamic) = 4–14 bits
- Sample rate:
  - 14 GS/s @ 4 bits
  - 7 GS/s @ 8 bits
  - 4 GS/s @ 14 bits
- Analog Input BW = 10.5 GHz
- Power dissipation = <½W (TBC)
- Footprint = TBD

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